Journal of Physical Sciences, Vol. 18, 2014, pp.54-61
ISSN: 0972-8791, www.vidyasagar.ac.in/journal
Published on 27th March 2014

An Efficient Design of True Single Phase Clocked Positive Latch Circuit Using Properly Sized MOSFETs and a Static Inverter to Accomplish Charge Storing Capacity During Low Activity Period of Clock Signal

Supratim Subhra Das[1] and Ria Das[2]
[1,2]Department of Electronics and Communication Engineering, Mallabhum Institute Of Technology, Bishnupur, Bankura-722122

Email: [1]supratim2014das@gmail.com, [2]riabose2014@gmail.com

Received on 26th February 2014; accepted on 25th March 2014.

ABSTRACT

For implementation of pipelined circuits, the roles of level-sensitive positive and negative latches are significant instead of edge-triggered registers. To avoid clock overlapping problem, true single phase clocked latches can be utilized which ensures correct pipeline operation. Therefore, in our design we have proposed a design of positive latch circuit controlled by single phase of a clock signal which help to hold the previous state of output without use of any capacitor in order to avoid the problem of capacitive coupling which is a major problem in most of the purely dynamic circuits. Although transistor sizing is very critical for achieving correct functionality of our design, but still to some extent proper sizing has been made with a sacrifice of not getting full swing at output.

1. Introduction

In digital circuitry, memories can be of two types – Static or Dynamic. Static memories store the state as long as the power is on. They are constructed by using positive feedback or regeneration, where the circuit topology consists of intentional connections between the output and the input of a combinational circuit. Static memories are most useful when the register will not be updated for extended period of time. Configuration data, loaded at power up time is a good example of static data. This condition also holds for most processors that use conditional clocking (i.e. gated clock) where the clock is turned off for unused modules. In that case, there are no guarantees on how frequently the registers will be clocked, & static memories are needed to preserve the state information. On the other hand, dynamic memories store data for a short period of time, perhaps milliseconds. They are based on the principle of temporary data storage on parasitic capacitors associated with MOS devices. Dynamic memories are basically simple with efficiently higher performance and lower power dissipation, but capacitors used in this need to be refreshed periodically to compensate for

charge leakage. Hence, they are most useful in datapath circuits which require high performance levels and periodically clocked circuits.

In our work, we suggest a positive latch circuit which can be used as an essential component of an edge-triggered dynamic register where positive latch can hold its previous state efficiently without the need of refreshment of capacitors to compensate for charge leakage, but that happens at the cost of loss of logic high value (i.e. 5 volt). Therefore, the availability of a high input impedance device for reading the value of stored signal from a capacitor without disrupting the charge is not mandatory. In our case logic high value is coming as 4.2 volt approximately and logic low value is coming as 0 volt.

2. Case Study

As mentioned in previous work [1], it is possible to design registers that only use single phase clock. The two single phase clocked register (TSPCR) proposed by Yuan and Svensson, uses a single clock. The basic single phase positive and negative latches are shown in Fig. 1 and Fig. 2.

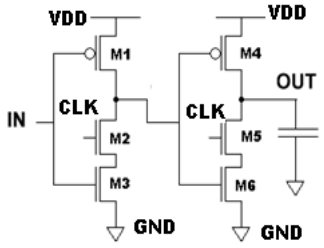

Figure 1: True single phase positive latch

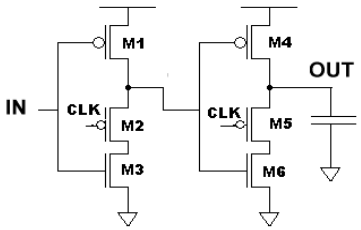

Figure 2: True single phase negative latch

For the positive latch, when clock is high, the latch is in the transparent mode and corresponds to two cascaded inverters; the latch is non-inverting, and propagates the input to the output. In other case when clock is low, both inverters are deactivated and the latch is in hold mode. Only the pull up networks is still active, while the pull down circuits is disabled. Here the clock load is similar to a conventional transmission gate register or C^2MOS register. The main advantage is the use of a single clock phase and the

disadvantage is the use of more number of transistors. A dynamic circuit in the style of Fig. 1 and Fig. 2 must be used with caution. When the clock is low (for the positive latch), the output may be floating, and it is exposed to coupling from other signals. Also, charge sharing can occur if the output node drives transmission gates. Dynamic nodes should be isolated with the aid of static inverters, or made pseudo static for improved noise immunity.

As with many other latch families, TSPC offers an additional advantage i.e. possibility of embedding logic functionality into the latches. This reduces the delay overhead associated with the latches. This approach of embedding logic into latches has been used extensively in the design of the EV4 Alpha microprocessor [2] and many other high performance processors.

According to [3], the TSPC latch circuits can be further reduced in complexity as illustrated in Fig. 3 and Fig. 4, where only the first inverter is controlled by the clock. This circuit has less number of transistors and the clock load is reduced by half.

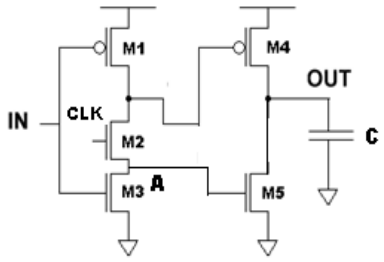

Figure 3: Simplified TSPC positive latch

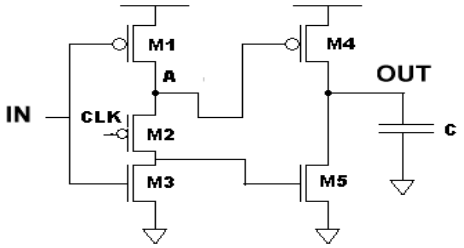

Figure 4: Simplified TSPC negative latch

One disadvantage of this circuit has been observed when it is simulated by Tanner Tool version 15.1. No previous state has been preserved for this circuit when clock goes low, although static inverter is used in second stage of this circuit as shown in Fig. 3 and Fig. 4. On the other hand, not all node voltages in the latch experience the full logic swing.

3. Software Issue

Tanner Tools Pro is a software suite for the design, layout and verification of analog, mixed-signal, RF and MEMS ICs. Tanner Tools Pro consists of fully-integrated front end and back end tools, from schematic capture, circuit simulation, and waveform probing to

physical layout. Tanner's fully-integrated solutions consist of tools for schematic entry, circuit simulation, waveform probing, full-custom layout editing, placement and routing, netlist extraction, LVS and DRC verification. Tanner EDA's innovative solutions are used in a range of applications in power management, next generation wireless, consumer electronics, imaging, biomedical, automotive and RF market segments.
Tanner EDA contains S-Edit™ schematic capture tool, T-Spice™ Circuit Simulator, L-Edit® and Hiper Verify®.
In our work we have used only S-Edit™ schematic capture tool and T-Spice™ Circuit Simulator.

Tanner's S-Edit™ schematic capture tool has been completely rearchitected and rebuilt into a new tool with user interface, performance and interoperability enhancements added. S-Edit supports integrated analog simulation with automatic conversion from Cadence® and ViewDraw® schematics. Users can run simulations and cross-probe from S-Edit, making the design process real-time and more efficient.The ability to view operating point simulation results directly on the schematic is another S-Edit productivity enhancing feature.

The T-Spice™ Circuit Simulator product delivers highly accurate results by supporting the latest foundry models, along with state-of-the-art numerical methods. T-Spice offers options and commands not found in Berkeley SPICE or most derivatives, such as design optimization, Monte Carlo analysis, multi-dimensional parameters, source and temperature sweeping. Tightly integrated with Tanner EDA's S-Edit schematic entry and W-Edit waveform probing tools, T-Spice provides the highest level of complexity for modeling and analysis.

Tanner EDA tool has been used in our work to implement digital circuit.The snapshot of schematic of the circuit as shown in Fig. 3 along with its transient response is given below

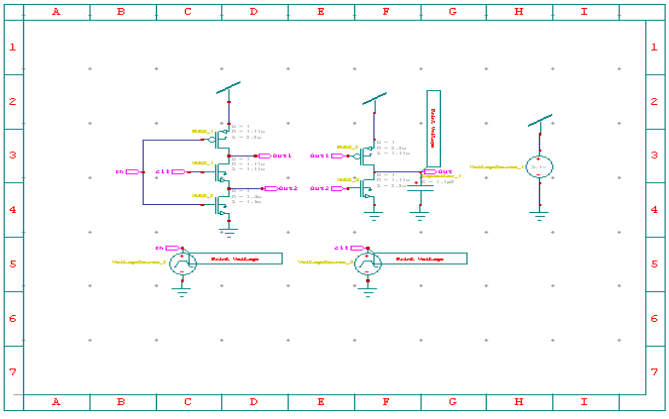

Figure 5: Snapshot of schematic of design in Fig. 3 implemented in Tanner S-Edit platform

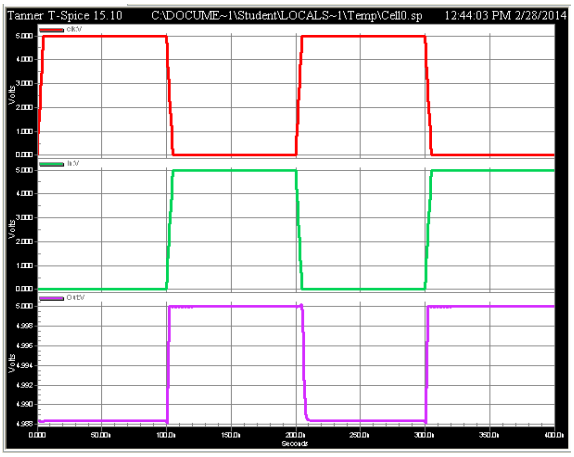

Figure 6: Snapshot of transient response of design in Fig. 3 obtained after T-SPICE simulation in Tanner EDA tool

For simulation, the transistor sizes are chosen as $(W/L)_{M1}$ = 0.11 μm / 2.2 μm, $(W/L)_{M2}$ = 0.11 μm / 0.11 μm, $(W/L)_{M3}$ = 0.3 μm / 0.9 μm, $(W/L)_{M4}$= 2.2 μm / 0.11 μm, $(W/L)_{M5}$ = 0.11 μm / 2.2 μm. The value of the capacitor used as load is 0.1 pF. The violet solid line represents the output waveform.
When input is low i.e. 0V, the voltage at node A for the positive latch maximally equals V_{DD} - V_{Tn}, which results in a reduced drive for the output NMOS transistor and a loss in performance. Similarly, same voltage at node A for negative latch can be driven down to | V_{Tp} | . This also limits the amount of V_{DD} scaling possible on the latch.

4. Proposed Work and Outcome

In our work, we propose a design of positive latch in which the previous state is preserved without the use of capacitor. Clock is connected to the gate of two MOSFETs, therefore clock load is two. The number of transistors used is six. A clocked inverter is cascaded with a static inverter as shown in Fig. 5.

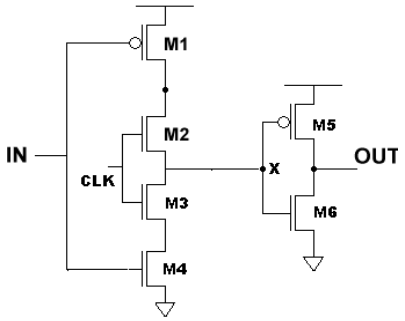

Figure 7: Proposed positive latch

An Efficient Design of True Single Phase Clocked Positive Latch Circuit using Properly Sized MOSFETs and a Static Inverter to Accomplish Charge Storing Capacity During Low Activity Period of Clock Signal

Transistor sizing is an important issue in our design. The channel width & channel length of PMOS and NMOS-es are so defined such that switching of latch can occur efficiently and previous state is successfully maintained. For a 0.25 μm CMOS technology, the following transistor sizes are selected: $(W/L)_{M1}$ = 0.5 μm / 0.5 μm, $(W/L)_{M2}$ = 0.35 μm / 0.35 μm, $(W/L)_{M3}$ = 0.45 μm / 0.5 μm, $(W/L)_{M4}$= 0.5 μm / 0.5 μm, $(W/L)_{M5}$ = 6 μm / 3 μm, $(W/L)_{M6}$ = 3 μm / 6 μm.

No static paths between V_{DD} and GND exist. One disadvantage of this circuit is unavailability of full logic swing. In this case, logic low value is obtained as zero volt, where logic high value is obtained as 4.2 volt. Another malfunction may occur when the slope of the clock is not sufficiently steep. Slow clocks cause both NMOS and PMOS clocked transistors to be on simultaneously, resulting in undefined values of the states and race conditions. The clock slopes should therefore be carefully controlled. If necessary, local buffers must be introduced to ensure the quality of the clock signals.
The snapshot of the schematic of design in Fig. 7 is given below along with its transient response.

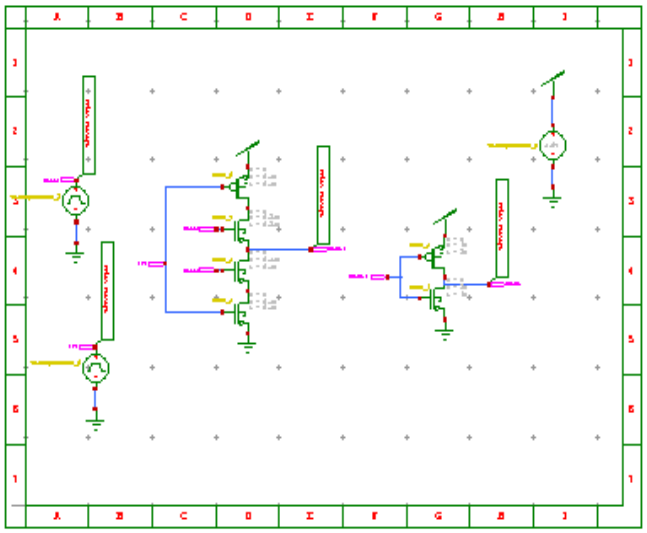

Figure 8: Snapshot of schematic of design in Fig. 7 implemented in Tanner S-Edit platform

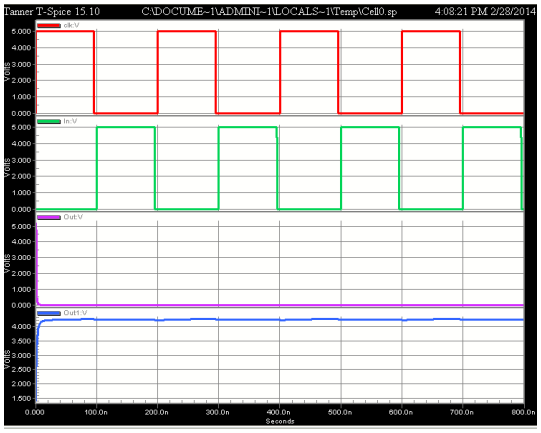

Figure 9: Snapshot of Transient response of design in Fig. 7 observed after T-SPICE simulation in Tanner EDA tool

The blue solid line represents the voltage waveform of intermediate node X of Fig. 7. The input parameters selected for above design are given below :
Input pulse width = 95 ns, Total time period of input pulse = 200 ns, delay = 100ns.
Clock pulse width = 95 ns, Total time period of clock pulse = 200 ns, delay = 0ns.
The blue solid line represents The following transient response has been obtained for the given input parameters: Input pulse width = 120 ns, Total time period of input pulse = 300 ns, delay = 150ns.

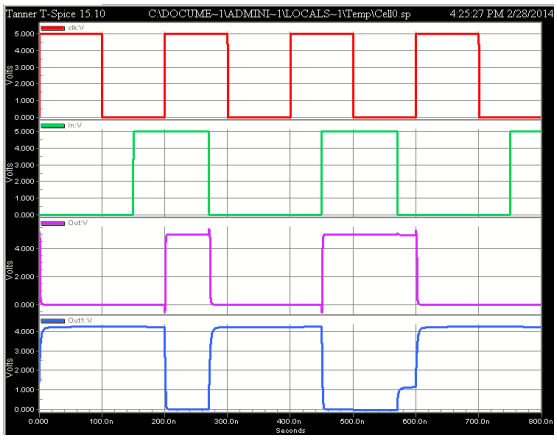

Figure 10: Another Snapshot of Transient response of design in Fig. 7 found after T-SPICE simulation in Tanner EDA tool

It is observed from both Fig. 9 and Fig. 10, when clock is high, then input is passed to the output and the value is retained until next high level of the clock appears.

5. Comparison with previous work

In fully dynamic circuit as shown in Figure, a signal net that is capacitively coupled to the output node can inject significant noise and destroy the state. This is especially important in ASIC flows, where there is little control over coupling between signal nets and dynamic nodes. Also leakage current is another problem. Therefore, for most modern processors, conservation of previous state or power is required in low activity periods of the clock.

On the other hand in our design there is no chance of such capacitive coupling to be occurred. Without use of capacitor previous state of the output can be retained by the virtue of proper transistor sizing use of properly sized static inverter .However, our circuit requires one extra transistors as compared to the Fig. 3 & Fig. 4, still this kind of positive latch being associated with another simplified negative TSPC latch resulting in an high performance edged triggered register can be used in a custom –designed high performance data path.

6. Conclusion

Nowadays pure dynamic memory circuits are hardly used anymore in spite of having reduced complexity higher performance and lower power consumption. Therefore in our work we have proposed a design which is having moderately high performance with high immunity against capacitive coupling and other sources of circuit induced noise. The combination of our proposed latch circuit with any other dynamic logic can produce fast computational circuit such as pipelined data path. Moreover, this proposed circuit without the use of static inverter at second stage can be used to construct edge-triggered register.

REFERENCES

1. J. Yuan and Svensson C., High –Speed CMOS Circuit Technique, IEEE JSSC, 24(1)(1989)62-70.
2. D. Dopperpuhl et al., A 200 MHz 64-b Dual Issue CMOS Microprocessor, IEEE Journal of Solid State Circuits,27(11)(1992)1555-1567.
3. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolić, Digital Integrated Circuits- A Design Perspective,by , Pearson Education, Inc., Upper Saddle River, New Jersey 07458, U.S.A.