M.Sc. 2nd Semester Examination, 2025

ELECTRONICS

(*Digital Circuit Laboratory*)

(Practical)

PAPER – ELC-205

Full Marks : 50

Time : 3 hours

Answer any **one** question selecting it by a **lucky draw**

1. Design and implement a half adder circuit using NAND gate only. Verify its truth table.

2. Design and implement a half adder circuit using NOR gate only. Verify its truth table.

3. Design and implement a Half subtractor circuit using NAND gate only and verify its truth table.

4. Design and implement a full adder circuit using NAND gate only and verify its truth table.

5. Design and implement a full adder circuit using 8 : 1 mux.

6. Design and implement a full adder circuit using 4 : 1 mux.

7. Design and implement 2-bit magnitude comparator circuit using basic gates.

8. Design and implement SR, JK flipflops using basic gates as well as with the help of an IC.

(*Continued*)

9. Design and implement : MOD 8 counter. Verify its states.

10. Design and implement : Binary to Gray code converter circuit.

11. Design and impement odd parity generator circuit.

Marks Distribution

Circuit design	:	15 Marks
Implementation	:	10 Marks
Results & Discussion	:	10 Marks
Viva-voce	:	10 Marks
LNB	:	05 Marks
Total	:	50 Marks