2025

M.Sc. 3rd Semester Examination

ELECTRONICS

Paper : ELC - 306

(VLSI Design Lab)

[Practical]

Full Marks : 50 Time : Three Hours

The questions are of equal value.

Answer any ***one*** question selecting it by lucky draw.

1. Draw a schematic diagram of a CMOS inverter circuit by using LT SPICE. Obtain the SPICE code of the circuit. Give the input and output waveforms of the circuit for transient analysis.

2. Draw a schematic diagram of a CMOS NAND gate by using LT SPICE. Obtain the SPICE code of the circuit. Give the input and output waveforms of the circuit for transient analysis.

3. Draw a schematic diagram of a CMOS NOR gate by using LT SPICE. Obtain the SPICE code of the circuit. Give the input and output waveforms of the circuit for transient analysis.

4. Draw layout of a CMOS inverter circuit by using layout design software. Give input and output waveforms.

5. Draw layout of a CMOS NAND gate by using layout design software. Give input and output waveform.

6. Draw layout of a CMOS NOR gate by using layout design software. Give input and output waveform.

7. Write Verilog code for half adder circuit. Create netlist. Obtain input-output waveforms.

8. Write Verilog code for full-adder circuit. Create netlist. Obtain input-output waveforms.

9. Write Verilog code for 4 : 1 Mux. Create netlist. Obtain input-output waveforms.

10. Write Verilog code for 3-bit synchronous counter. Create netlist. Obtain input-output waveforms.

11. Draw a CMOS inverter circuit. Obtain SPICE code for the circuit. Give the input-output waveforms for the DC analysis of the circuit.

12. Write Verilog code for $y = A(B + C)$. Create netlist. Obtain input-output waveforms.

Distribution of Marks

Program : 10 Marks

Execution : 15 Marks

Results : 10 Marks

Viva-voce : 10 Marks

Laboratory Notebook : 05 Marks

Total : 50 Marks
