2025

M.Sc. 3rd Semester Examination

ELECTRONICS

Paper : ELC - 302

(VLSI Design and Technology)

Full Marks : 50 Time : Two Hours

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

Group - A

Answer any ***four*** questions : 2×4=8

1. What do you understand by design hierarchy in VLSI systems?
2. Draw a schematic diagram of an n-channel depletion MOSFET.
3. What are short channel and narrow channel MOSFETs? 1+1
4. Define class 100 clean room.
5. Why do we need IC packaging?
6. Describe CMOS digital logic design.

P.T.O.

Group - B

Answer any *four* questions : 4×4=16

7. Explain the concept of regularity, modularity and locality in VLSI design approach.

8. Draw and explain MOS C-V characteristics.

9. Draw a diagram for various charges associated with thermally oxidized silicon. How can be they minimized? 1+3

10. Why do we need silicon nitride deposition in IC fabrication? Describe the processes to grow silicon nitride films. 1½+2½

11. Describe how the NMOS devices be used as switches. Derive the expression for MOS on resistance. 2+2

12. Define fan-in and fan-out. Calculate the noise margins of a logic gate having $V_{out} = 5V$, $V_{IH} = 2.5V$ and $V_{IL} = 0.8V$, where the symbols have their usual meanings. (1+1)+2

Group - C

Answer any *two* questions : 8×2=16

13. What are the different methods of producing the image of a mask on a wafer? Briefly discuss the methods. 2+6

14. Discuss with diagrams the steps followed in the fabrication of an enhancement mode n-MOSFET. 8

15. Show how a parasitic transistor is formed in a CMOS structure. What is latchup? How is it prevented? 3+3+2

16. Develop the CMOS circuit for a full adder with explanation. 5+3

[Internal Assessment - 10 marks]
