Journal of Physical Sciences, Vol. 12, 2008, 213-220

Design of a Phase Detector with Improved Performance

B. Chakraborty and R.R. Pal
Department of Physics and Technophysics
Vidyasagar University, Midnapore 721 102 (W.B.) India
e-mail : radha_raman_pal@yahoo.com

Received November 30, 2008; accepted December 15, 2008

ABSTRACT

This paper presents a new type of bipolar analog Phase Detector (PD) using a high speed low voltage Emitter Coupled Logic (ECL) inverters, where positive feedback has been introduced to increase the operating range. Introduction of positive feedback has also reduced the supply voltage requirement. The same technique has been introduced in a NMOS Gilbert phase detector and similar results were obtained. The minimum supply voltage required for both these circuits were 2.1 volts.

Keywords: *Phase Detector (PD), Voltage Controlled Oscillator (VCO), Emitter Coupled Logic (ECL), Phase Locked Loop (PLL).*

1. Introduction

The recent developments of telecommunication systems has brought an increased demand for low-jitter, high-speed phase-locked loops (PLL). The phase detector is a key element in PLLs and has from a historical point of view not been able to handle large input frequency differences [1]. The phase detector compares the phase of a periodic input signal against the phase of the output of VCO, and generates an average output voltage V_{out}, which is linearly proportional to the phase difference, $\Delta\phi$, between its two inputs. In the ideal case, the relationship between V_{out} and $\Delta\phi$, is linear, crossing the origin for $\Delta\phi = 0$[2] . The output voltage of the phase detector is a D.C voltage and therefore is often referred to as the error voltage. The output of the phase detector is often applied to a low-pass filter, which removes the high frequency noise and produces a D.C level. This D.C level, in turn, is the input to the voltage controlled oscillator (VCO) of a PLL. The filter also helps in establishing the dynamic characteristics of the PLL circuit- the VCO frequency is compared with the input frequencies and adjusted until it is equal to the input frequencies.

$$\text{Let } V_x = E_x \text{Cos}\omega t, \text{ and } V_y = E_y \text{Cos}\left(\omega t + \varphi\right)$$

$$V_{out} = V_x V_y = KE_x E_y \text{Cos}\omega t \, \text{Cos}\left(\omega t + \varphi\right)$$

$$= \frac{KE_x E_y}{2}\left[\text{Cos}\varphi + \text{Cos}\left(2\omega t + \varphi\right)\right]$$

Using low pass filter at the output removes the double frequency term and the resulting output will be proportional to the cosine of the phase difference. Where K is a constant and ϕ is the phase difference between the two input signals.

The simplest example of digital phase detector is an exclusive OR, XOR gate. The width of the output pulses varies with the phase difference between the inputs that providing a dc level proportional to $\Delta\phi$. The error pulses on both rising and falling edges can be produced by the XOR circuit, but other types of PD only respond to positive or negative transitions.

This paper presents an analog Phase Detector (PD) using a high speed low voltage Emitter Coupled Logic (ECL) inverters. Positive feedback has been introduced to increase the operating range of the PD and to reduce the supply voltage requirement of the PD.

2. Calculation of phase detector output using hybrid Π–parameter

The circuit diagram of a conventional phase detector is given the Figure 1. We have introduced a positive feedback scheme in the phase detector to improve its performance[3].

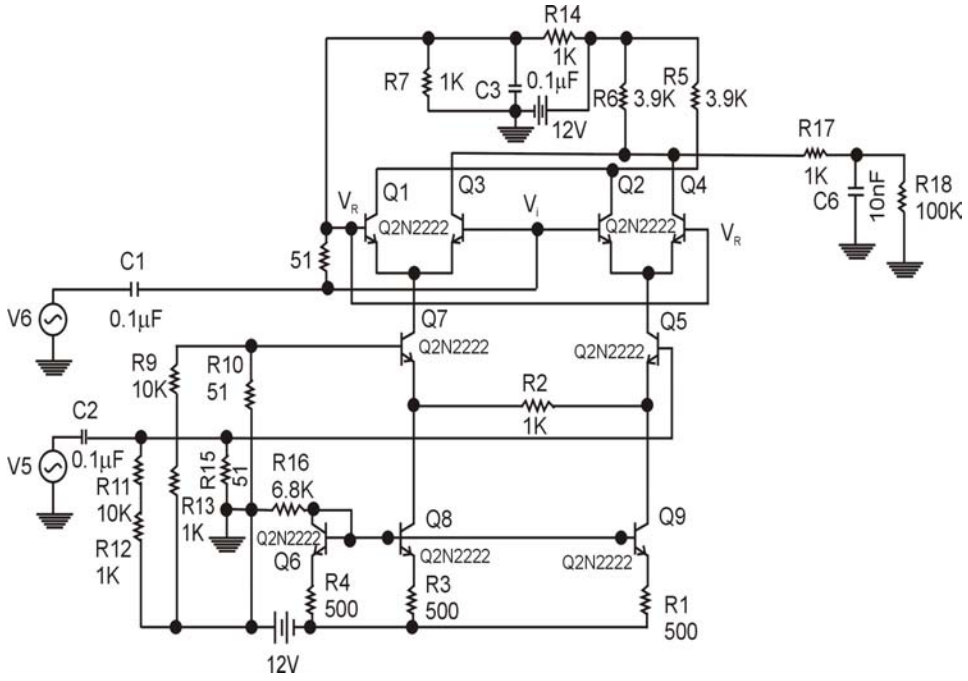

Fig. 1. Conventional Phase detector.

A simple circuit of the PD using ECL inverter (single stage) is shown in Figure 2.

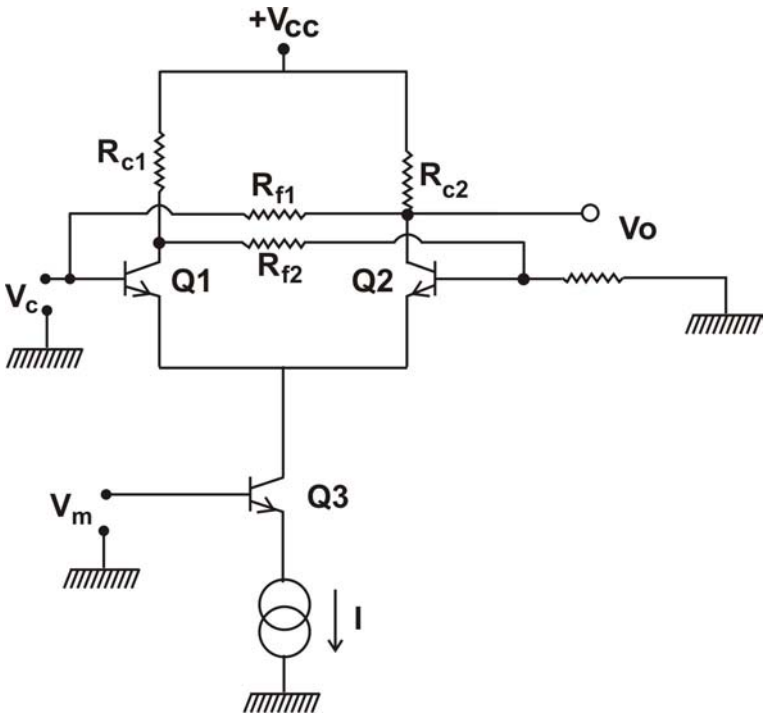

Fig. 2. Simple Phase Detector circuit using ECL inverter with positive feedback.

An A.C small signal equivalent circuit of Figure 2 using hybrid-□ parameters with positive feedback is shown in Figure 3.

2.1 Calculation of output voltage without positive feedback i.e. in absence of R_{f1} and R_{f2}

It has been shown in [3] that the output voltage of the circuit of figure 3 is,

$$V_{out} = \left[\frac{\beta_{01} R_{c1}}{r'_{\pi 1} + r_{x1}}\right] \times \left[\frac{r'_{\pi 3} + (1+\beta_{03})R}{r'_{\pi 3} + r_{x3} + (1+\beta_{03})R}\right] V_c V_m$$

$$= \text{Constant} \times V_c V_m$$

where, $\text{Constant} = \left[\frac{\beta_{01} R_{c1}}{r'_{\pi 1} + r_{x1}}\right] \times \left[\frac{r'_{\pi 3} + (1+\beta_{03})R}{r'_{\pi 3} + r_{x3} + (1+\beta_{03})R}\right]$

Hence we the output is directly proportional to the product of the carrier and modulating voltage.

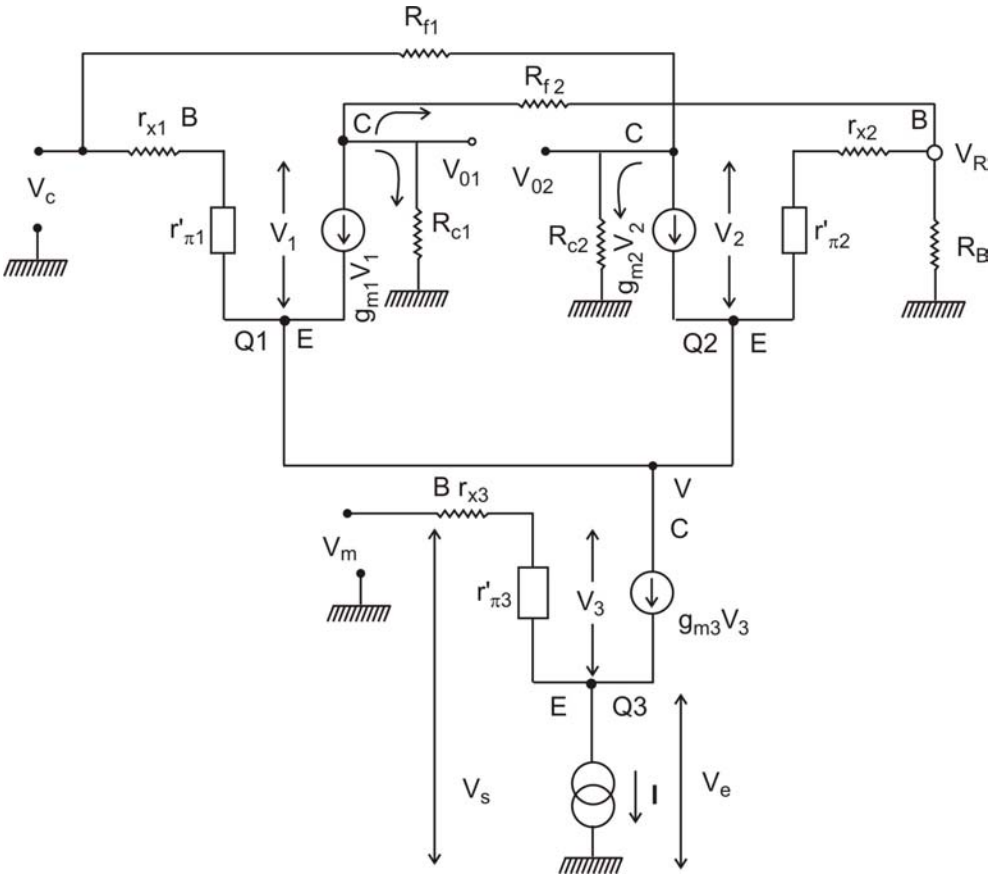

Fig. 3. A.C small signal equivalent circuit of Fig. 2 with positive feedback**.**

2.2 Calculation of output voltage with positive feedback

From the circuit of Figure 3 we can write,

$$V_{01} = \frac{\left[\frac{V_R}{R_{f2}} + g_{m1} I_{b1} r'_{\pi 1}\right] R_{c1}}{\left[1 + R_{c1}/R_{f2}\right]}$$

$$= \frac{\frac{V_R R_{c1}}{R_{f2}} + g_{m1} I_{b1} r'_{\pi 1} R_{c1}}{1 + R_{c1}/R_{f2}}$$

Here, V_R is the reference voltage, effectively V_R=0, Hence

$$V_{01} = \frac{g_{m1} I_{b1} r'_{\pi 1} R_{c1}}{1 + R_{c1}/R_{f2}}$$

If R_{c1} =1kΩ and R_{f2} = 4.7 kΩ, then $R_{c1}/R_{f2} = 0.213$

Again R_{c1} =1kΩ and R_{f2} = 10 kΩ, then $R_{c1}/R_{f2} = 0.1$

Hence we can conclude that if feedback resistance R_{f2} is decreased, the output voltage also decreases. In other words, to get the same output voltage the phase difference of the two input signals should be increased, i.e. the locking range increases with the decrease of feed back resistance. This expression is also valid for V_{02}.

3. Phase Detector using NMOS technology

The circuit shown in figure 1 can also be realized using NMOS technology. The modified circuit diagram using NMOS transistors is shown in figure 4. This is a Gilbert Phase Detector [1]. The same positive feedback technology can be applied to this NMOS phase detector to increase its performance range. A simplified form of this circuit using positive feedback has been represented in figure 5.

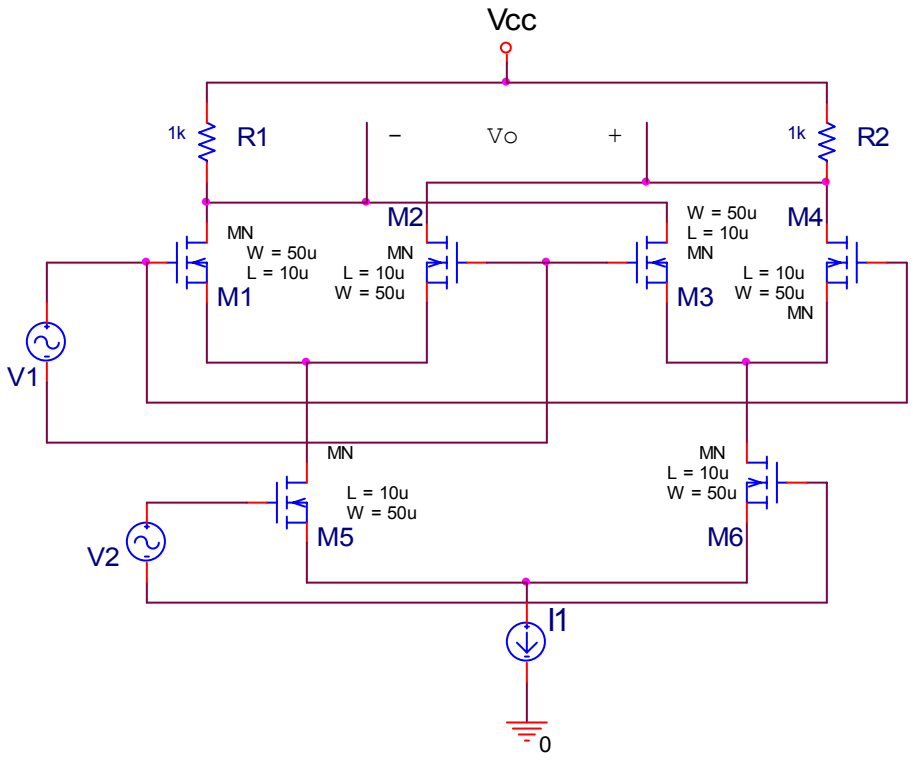

Fig. 4. A Gilbert Phase Detector using NMOS transistors.

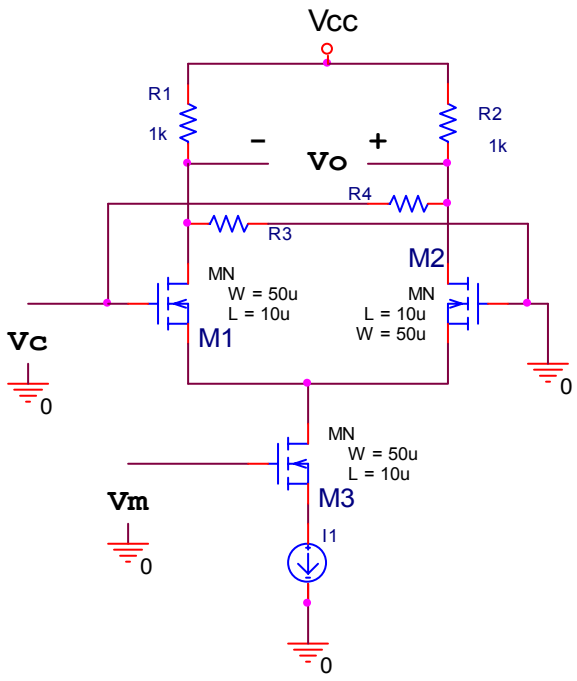

Fig. 5. Simple Phase Detector circuit using NMOS transistors with positive feedback.

4. Experimental Results and Discussions

The phase detector circuit shown in figure 5 was simulated using the circuit simulation programme PSPICE and the simulated variation of phase detector output as a function of input phase difference for different amounts of feedback is shown in figure 6. The results show that with the introduction of positive feedback, the phase detector output decreases. From this graph we see that with the introduction of 4.7kΩ feedback resistance, the output voltage of the phase detector decreases by about 14%. Also for a fixed value of the feedback resistance the phase detector output decreases approximately linearly when the phase difference between the two input signals change from 0 to π radians. On the other hand the output voltage increases approximately linearly when the phase difference between the two input signals change from π to 2π radians. Figure 7 shows the simulated output waveforms of the NMOS phase detector shown in figure 5. This figure indicates that the two input signals are being multiplied at the output.

5. Conclusion

In this paper we have reported the results of the performance of a phase detector using NMOS transistors. Positive feedback has been introduced in the Gilbert phase detector. Results show that the input phase difference range has been increased by approximately 14 % compared to the phase detector without feedback. The required minimum supply voltage was 2.1 volts.

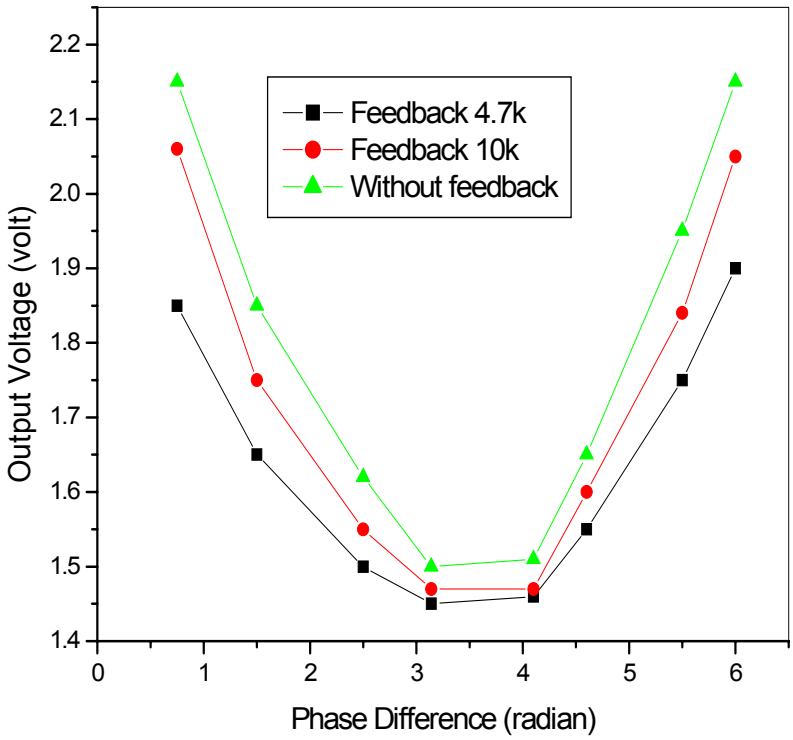

Fig. 6. Simulated graph of phase detector output with input phase difference.

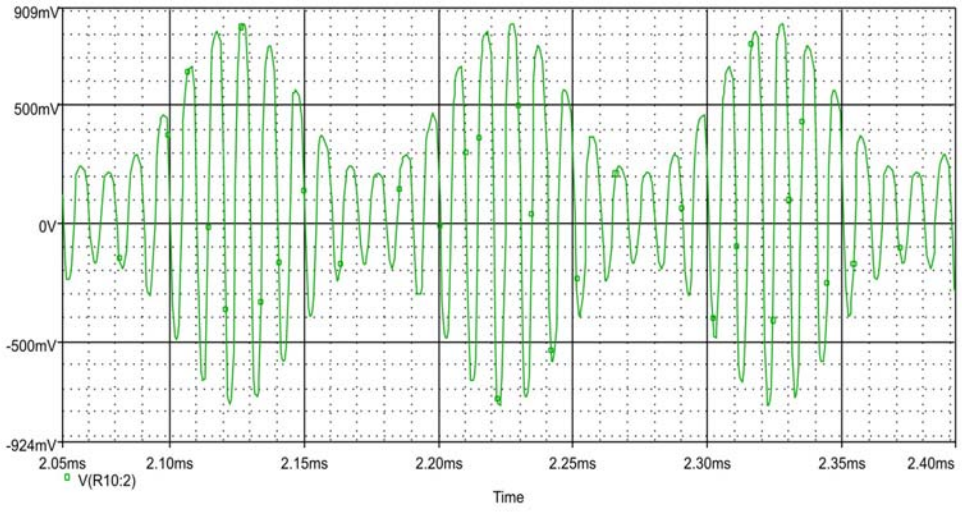

Fig.7. Simulated output waveform of the single stage Phase Detector of the circuit of Fig. 5.

REFERENCES

1. S. Soliman F. Yuan and K.Raahemifar, *An Overview of Design Techniques for CMOS Phase Detectors,* IEEE Circuit and Systems, (2002), 457-460.
2. B. Razavi, *Design of Analog CMOS Integrated Circuits*,. McGRAW-HILL, (2001).
3. B. Chakraborty and R.R. Pal, *Design of a PLL with improved locking range and its biomedical applications*, International Journal of Electronics, Vol. 94, No. 7, (2007), 671-682.