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Synchronous Oscillator Using High Speed Emitter Couple Logic (ECL) Inverters

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ABSTRACT

This paper presents a synchronous oscillator using a high speed low voltage Emitter Coupled Logic (ECL) inverter. Using the positive feedback the locking range increases, compared to the oscillator without any positive feedback. A maximum improvement (increase) of locking range of around 172% was obtained from circuit simulation as well as from practical circuit, using discrete components. Here the supply voltage requirement is 2.1 volts.

Key words : *Synchronous Oscillation (SO), Voltage Controlled Oscillator (VCO), Current Controlled Oscillator (CCO), Ring Oscillator, Emitter Coupled Logic (ECL).*

1. Introduction

The Synchronous Oscillator (SO) is a free-funning Oscillator which oscillates at its natural frequency in the absence of an externally applied signal. In the presence of a signal, the oscillator synchronizes with and tracks the input wave form with an acquisition time inversely proportional to the tracking band width. The acquisition time of the synchronous oscillator is considerably smaller then that of conventional PLLs, which are limited by the trade off between noise rejection and acquisition time in the loop filters [1]. The synchronous oscillator possesses a constant output signal amplitude in the tracking region and an adaptive tracking band width proportional to the input signal level. A decrease in the input carrier-to-noise ratio reduces the SO's tracking band width to maintain a constant carrier-to-noise ratio at the SO's output. A SO can track signals which have very low carrier to-noise ratio. So the noise rejection properties of the SO is very high [2].

The synchronization is applied to frequency modulation recevers [3-4] and carrier-communication systems [5-6]. Also the synchronized oscillator can be used as an F-M discriminator-demodulator by coupling an auxiliary resonant circuit to the test

oscillator and injecting the synchronizing signal into this auxiliary circuit [7]. In the application of F-M synchronous amplifier limiter, the oscillator is locked to an F.M. signal. Note that the properties of the external source, supplying the synchronizing signal and the coupling impedance, are important in determining the band width and phase of synchronization.

It is more effective for locking range to even harmonics, because when the oscillator oscillates at its free running frequency f_{free}, the voltage developed at the current source point Q will have a frequency equal to $2f_{free}$. So it is expected that if the signal be injected at the current source node P the locking range will be more at $2f_{free}$ and for all even harmonics. Also due to the application of positive feedback the delay time produce by each inverter reduces and the oscillation frequency of the ring VCO increases [8]. So the locking range also increases by proportional amount.

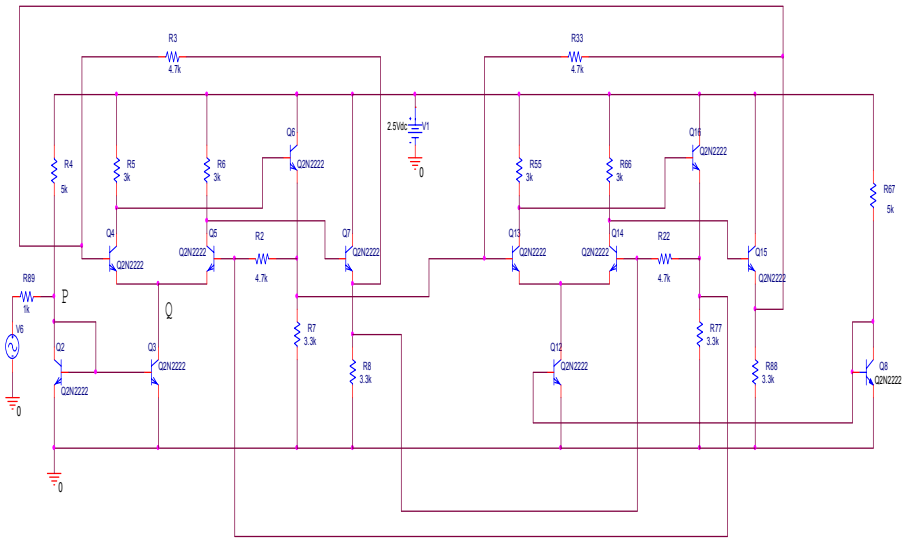

Fig.1 : Synchronous Oscillator using modified ECL inverter.

2. Experimental Results and Discussions

The variation of locking range with input voltage for different feedback resistances are shown in Fig. 2. The variation of input voltage is 0.5-2.0 volts because the circuit can operate the maximum supply voltage 2.1 volts.

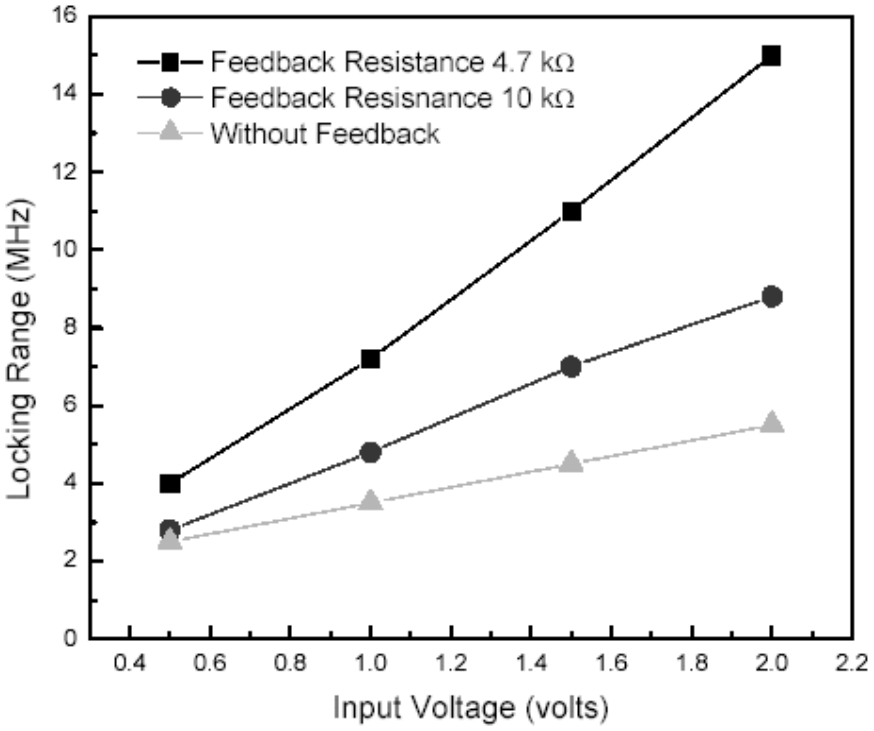

Fig.2 : Variation of locking range with input voltage for different feedback resistances.

The experimental result shows that the maximum locking range is15MHz for feedback resistance of 4.7 kΩ, in contrast to the maximum locking range of only 5.5MHz for synchronous oscillator without any positive feedback.

Fig.3 shows the input and output signals of the synchronous oscillator and fig.4 shows the waveforms of the input noise signal (upper wave) and noise suppressed output signal (lower wave) for synchronization at a frequency of about 56MHz. The output signal of the synchronous oscillator is almost noise free.

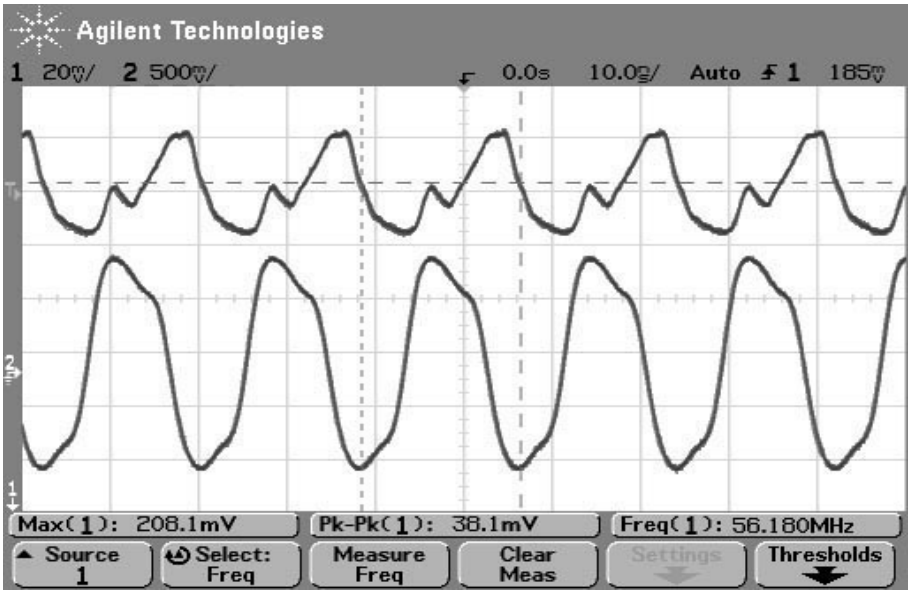

Fig.3 : Photograph of the input and output signals of synchronous oscillator (Upper- Output waveform, Lower- Input waveform)

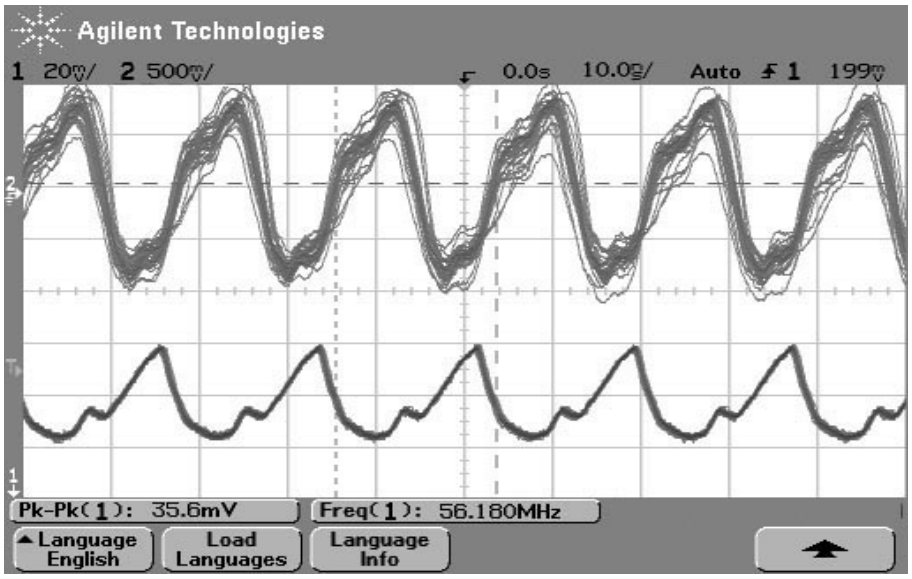

Fig4 : Photographs of the wave forms of the input noise signal (upper wave) and noise suppressed output signal (lower wave) of frequency 56.180MHz.

3. Conclusion

In this paper, a synchronous oscillator has been realised using ECL inverters with positive feedback. Introduction of positive feedback increases the locking range by amount 172% compared to the synchronous oscillator realised without any positive feedback. The locking range is maximum for 4.7 kΩ feedback resistance with input voltage 2.1 volts. Due to the positive feedback the delay time reduces and oscillation frequency of the ring VCO increases. Hence the locking range also increases proportionally.

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