M. Sc. 3rd Semester Examination, 2023

ELECTRONICS

(*VLSI Design and Technology*)

PAPER – ELC-302

Full Marks : 50

Time : 2 hours

The figures in the right hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

GROUP – A

Answer any **four** of the following questions : 4×2

1. What is design hierarchy? 2

2. Compare the performances of *n*-channel and *p*-channel MOSFETs. 2

3. What do you mean by short channel and narrow channel? 1 + 1

4. Mention basic steps in IC fabrication. 2

5. List the advantages of retrograde well. 2

6. What is CMOS transmission gate? 2

GROUP – B

Answer any **four** of the following questions : 4 × 4

7. What do you mean by MOSFET scaling? Describe the different types of scaling techniques. 1 + 3

8. Derive the expression for drain current (I_D) in a MOSFET. 4

9. Define a class 100 clean room. If we expose a 200 mm wafer for 1 minute to an air steam under a laminar-flow condition at 30 m/min, how many dust particles will fall on the wafer in a class 10 clean room? 2 + 2

10. Describe an ion implantation system with a schematic diagram. 4

11. "MOS transistor acting as a switch"- Explain. 4

12. Explain CMOS logic design. A logic gate has $V_{OH} = 5V, V_{OL} = 0.2V, V_{IH} = 2.5V$ and $V_{IL} = 0.8V$. Calculate the noise margins (Symbols have their usual meanings). 2 + 2

GROUP – C

Answer any **two** of the following questions : 2 × 8

13. Describe with a diagram various capacitances in MOSFET. 5 + 3

14. What are the advantages of ion implantation over a diffusion process ? List the problems involved in ion implantion. How can they be solved? $2\frac{1}{2} + 2\frac{1}{2}$

15. Show how a parasitic transistor is formed in a CMOS structure. What is latchup? How is it prevented? 3 + 3+2

16. Describe CMOS design methodology for digital circuits. Implement the function $F = \sum m(0,1,2,4,6,8,10,12,14)$ using CMOS logic. 3 + 5

[Internal Assessment – 10 Marks]
