2022

MCA

2nd Semester Examination

ADVANCED COMPUTER ARCHITECTURE

PAPER—MCA-201

Full Marks : 100

Time : 3 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Group—A

1. Answer any *five* questions : 5×2

(a) What is the difference between asynchronous and synchronous pipeline ?

(b) What is Von Neumann bottleneck?

(c) State four features of RISC.

(d) What is Flynn's classification of computer?

(e) Compare write-through and write-back policy.

(f) Distinguish between logical and arithmetic shift operations.

(g) What is vector processor?

(h) What is reservation table in pipeline?

Group—B

Answer any *four* questions. 4×15

2. (a) What is pipelining?

(b) Determine clock period of a 3-stage linear pipeline unit where stage delays of three stages are 5 ns, 10 ns and 7 ns and latch delay is 2 ns.

(c) Explain different type of data hazards.

(d) How can we reduce control hazard ?

2+4+6+3

3. (a) Find the maximum efficiency of a k-stage pipeline unit.

(b) Consider a 4-stage pipeline processor with clock rate of 5 MHz. Obtain the clock period. Calculate speed up, efficiency and throughput for 1000 instructions. 5+(2+3+3+2)

4. (a) Compare Von Neumann and Harvard architecture.

(b) Explain micro programmed control unit with diagram.

(c) Explain the roles of device interface and driver.

(d) Distinguish between RISC and CISC.

3+5+4+3

5. (a) Explain SIMD architecture.

(b) Explain NUMA model of multiprocessor.

(c) What is the difference between NUMA and COMA model of multiprocessor ? 6+5+4

6. (a) Briefly explain hierarchical memory organization.

(b) Explain inclusion, coherence, locality of reference properties of memory hierarchy.

6+(3+3+3)

7. (a) Explain the terms : Hit ratio, Access frequency and average access time.

(b) How can we determine the cost of a memory hierarchy ?

(c) A three level memory system having cache access time of 15 ns, disk access time of 80 ns has a cache hit ratio of 0.96 and main memory hit ratio of 0.9. What should be the main memory access time to achieve average access time of 25 ns ? 6+3+6

8. Consider the following reservation table of a non-linear pipeline processor for function P :

		Clock →							
		1	2	3	4	5	6	7	8
Stages	S_1	P					P		P
	S_2		P		P				
	S_3			P		P		P	

(a) Find out all forbidden and non-forbidden latencies.

(b) Obtain the initial collision vector.

(c) Draw state transition diagram.

(d) List all simple and greedy cycles.

(e) Calculate minimal average latency.

4+2+5+2+2

9. Write short notes of the following :

(a) Carry propagate adder ;

(b) Paging ;

(c) Latency sequence, latency cycle and constant cycle in pipeline ;

(d) Direct mapping technique. 4×5

[Internal assessment - 30]

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