2018

CBCS

3rd Semester

PHYSICS

PAPER—C7P

(Honours)

(Practical)

Full Marks : 20

Time : 2 Hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Digital Systems and Applications Lab.

Write an experiment (any *one*) : 1×15

1. Design a NOT gate using transistor and verify the truth table.

(a) Theory 5

(b) Showing the result and noting the truth table. 8

(c) Results and discussions. 2

2. Design and verify AND, OR, XOR gates using NAND gate ICs.

   (a) Theory 2+2+2

   (b) Noting the truth table and showing the result. 2+2+2

   (c) Results and discussions. 3

3. Convert the following Boolean expression into logic circuit and design it using logic gate ICs.

$$y = \sum_{m}(1,3,5,7)$$

   (a) Theory 6

   (b) Showing the result and noting the truth table. 7

   (c) Results and discussions. 2

4. Design a 4 bit binary adder and check the result for 3 data set.

   (a) Theory 6

   (b) Showing the result and noting the truth table. 7

   (c) Results and discussion 2

5. Design an adder subtracter circuit using full adder IC and check both the result of addition and subtraction for 2 data set.

   (a) Theory 6

   (b) Showing the result and noting the truth table. 7

   (c) Results and discussions. 2

6. Design a RS flip-flop using NAND gates and demonstrate the excitation table.

   (a) Theory 6

   (b) Showing the result and noting the truth table. 7

   (c) Results and discussions. 2

7. Design a JK flip-flop using NAND gates and demonstrate the excitation table.

   (a) Theory 6

   (b) Showing the result and noting the truth table. 7

   (c) Results and discussions. 2

8. Design a JK Master-slave flip-flop using NAND gate ICs and demonstrate the excitation table.

   (a) Theory 6

   (b) Showing the result and noting the truth table. 7

   (c) Results and discussions. 2

9. Design a 4 bit counter using JK flip-flop ICs and study the timing diagram.

   (a) Theory 6

   (b) Showing the result and noting the truth table. 7

   (c) Results and discussions. 2

10. Design a 4 bit shift register SIPO using D-type/JK flip-flop ICs.

    (a) Theory 6

    (b) Showing the result and noting the truth table. 7

    (c) Results and discussions. 2

11. Design a 4 bit shift register PISO using D-type/JK flip-flop using ICs.

    (a) Theory 6

    (b) Showing the result and noting the truth table. 7

    (c) Results and discussions. 2

12. Design an astable multivibrator at frequency 10 KHz with 2/3-rd duty cycle using 555 timer IC.

    (a) Theory 6

    (b) Showing the result and noting the truth table. 7

    (c) Results and discussions. 2

13. Design a monostable multivibrator using 555 timer IC with ON times 20 sec and 50 secs.

    (a) Theory 6

    (b) Showing the result and noting the truth table. 7

    (c) Results and discussions. 2

Distribution of Marks :

LNB–02; Viva–03; Experiment–15