2019

B.Sc.

3rd Semester Examination

PHYSICS (Honours)

Paper - C 7-T

(Digital System and Applications)

Full Marks : 40 Time : 2 Hours

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

1. Answer any *five* questions of the following : 5×2=10

   (a) Write down advantages of Integrated Circuits.

   (b) What do you mean by positive logic and negative logic.

   (c) Convert hexadecimal number $(2F9A)_{16}$ to equivalent binary number.

(d) Prove that negative logic OR gate is equivalent to positive logic AND gate.

(e) Write down SOP expression for the Booleau function

$$f(A, B, C, D) = \sum m(0, 3, 6, 7, 10, 12, 15).$$

(f) What is Race-around condition in J-k Flip-Flop.

(g) Draw half adder circuuit using NAND gates only.

2. Answer any *four* qustions : 4×5=20

(a) (i) Design a positive logic NOT circuit using transistor.

(ii) How OR gate can be constructed using transistors only ? 3+2

(b) Minimize the Boolean function $f(A, B, C, D)$.

$= \sum m(0, 1, 2, 3, 11, 12, 14, 15)$ by karnaugh map. 5

(c) Explain why NAND gate is called Universal Gate. Construct $EX-OR$ Gate using NAND Gates only. 3+2

(d) Add the binary numbers 1111, 0111, 1011 and 1001. Perform the binary subtract 1000–1001 using 2's complement method. 2+3

(e) Construct a 4-bit full adder circuit using half adders only. 5

3. Answer any *one* question. 1×10=10

(a) (i) Implement the Boolean expression

$$f(A, B, C, D) = \sum m(0, 2, 3, 6, 8, 9, 12, 14)$$

(ii) Design a 1 : 4 demultiplexer. 6+4

(b) (i) Draw the circuit diagram of a Master-Slave J-K Flip-Flop and explain its operation.

(ii) Design a monostable multivibrator using IC 555. 5+5