B.Sc.-CBCS/IS/COS/H/C2P
(Set-1)/17(Pr.)

2017

COMPUTER SCIENCE

[Honours]

(CBCS)

(Practical)

PAPER – C2P(Set-1)

Full Marks : 20

Time : 2 hours

The figures in the right hand margin indicate marks

[Set–1]

GROUP – A

Answer any **one** questions : 10 × 1

1. Design and implement a D flip-flop.

2. Design and implement a JK flip-flop.

3. Design and implement a full adder circuit using NAND gates only.

4. Design and implement a 3 × 8 decoder.

5. Design and implement a 8 bit parity generator.

6. Design and implement of a 4 bit adder.

7. Design and implement a 4 bit counter.

8. Design and implement a two bit digital comparator.

9. Design and Implement a 8 : 1 multiplexer.

10. Design and implement a half-subtractor using NAND gates only.

GROUP – B

Answer any **one** question : 5 × 1

Consider the diagram in Fig. 1(attached here with) answer the following questions :

Register Set

IR	DR	AC	AR	PC	FGI	FGO	S	I	E
0 15	0 15	0 15	011	011	1 Bit	1 Bit	1 Bit	1 Bit	1 Bit

Memory	Instruction format
4096 words 16 bits per word	0 3 4 15 Opcode | Address

Basic Computer Instructions

Memory Reference			Register Reference		Input-Output		
Symbol	Hex		Symbol	Hex	Symbol	Hex	
AND	0xxx	Direct Addressing	CLA	E800	INP	F80 0	Optional
ADD	2xxx		CLE	E400	OUT	F40 0	
LDA	4xxx		CMA	E200	SKI	F20 0	
STA	6xxx		CME	E100	SKO	F10 0	
BUN	8xxx		CIR	E080	ION	F08 0	
BSA	Axxx		CIL	E040	IOF	F04 0	
ISZ	Cxxx		INC	E020			
AND_I	1xxx	Indirect Addressing	SPA	E010			
ADD_I	3xxx		SNA	E008			
LDA_I	5xxx		SZA	E004			
STA_I	7xxx		SZE	E002			
BUN_I	9xxx		HLT	E001			
BSA_I	Bxxx						
ISZ_I	Dxxx						

Fig. 1

11. Create a Fetch routine of the instruction cycle.

12. Simulate the machine to determine the contents of AC, E, PC AR and IR registers in hexadecimal after the execution of each of the following register reference instructions.

    (*a*) CLA

    (*b*) HLT.

$$\begin{bmatrix} \text{PNB} - 2 \\ \text{VIVA} - 3 \end{bmatrix}$$