2018

CBCS

1st Semester

COMPUTER SCIENCE

PAPER—C2T

(Honours)

Full Marks : 40

Time : 2 Hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Computer System Architecture

Group—A

1. Answer any *five* questions. 5×2

(a) Give the truth table of 2-input NAND gate.

(b) Give the characteristic table of J-K flip-flop.

(c) Add the following two numbers and write the result in Hexa-decimal base : $(ABEF)_H + (234)_H$.

(d) Simplify the following Boolean expression using Karnaugh map :

$$F = ABC + A\overline{B}C + \overline{A}\overline{B}D + \overline{A}BCD .$$

(e) How do we detect overflow condition after an ALU operation in an 8-bit CPU ?

(f) What is the role of Instruction Register in CPU ?

(g) To interface a memory of size 2 KB with a CPU, what should be the minimum size of address bus ?

(h) What do you mean by direct addressing mode ?

Group—B

2. Answer any *four* questions : 4×5

(a) (i) What is the role of accumulator register in ALU ?

(ii) Evaluate the following arithmetic expression using 1-address instructions and 0-address instructions only :

$$X = (A - B) * (C - D)$$

where A, B, C, D, X are CPU registers. 1+4

(b) (i) How does hardwired control unit differ from Microprogrammed control unit ?

(ii) Why microprogrammed is so called 'micro' ?

3+2

(c) (i) Realize EX-OR gate using NAND gates only.

(ii) How does sequential circuit differ from combinational circuit ? 3+2

(d) (i) Construct the T F/F from J-K F/F.

(ii) Construct a 3×8 decoder using two 2×4 decoders. 2+3

(e) Design a 3-bit left shift register using J-K flip-flop.

(f) Briefly explain the working of Interrupt-driven I/O.

Group—C

3. Answer any *one* question : 1×10

(a) (i) Design a 1-bit ALU that supports the following arithmetic and logic operations :

Addition, Subtraction, NAND and EX-OR.

(ii) How do we represent floating-point numbers in IEEE 754 notation ?

(iii) What do you mean by instruction execution cycle ? 4+3+3

(b) (i) We have to interface four 1 KB memory chips with a CPU with 16-address lines. Show the interfacing of these memory chips with CPU. Also derive the resultant memory address map of the 4 KB memory.

(ii) What do we mean by cache miss?

(iii) Show the representation of negative number $-(21)_{10}$ using 2's complement representation in an 8-bit register? (4+2)+2+2

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