2018

CBCS

1st Semester

COMPUTER SCIENCE

(Honours)

PAPER—C2P

(Practical)

Full Marks : 20

Time : 2 Hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Set–1

Answer any *one* question (Lottery basis).

1. Design and implement a 8 : 1 multiplexer.

2. Design and implement a half subtractor using NAND gates only.

3. Design and implement a 8 bit parity generator.

4. Design and implement a D flip-flop.

5. Design and implement a 3×8 decoder.

6. Design and implement a JK flip-flop.

7. Design and implement a 4 bit synchronous counter.

8. Design and implement a full adder circuit using NAND gates only.

9. Design and implement a 4 bit adder using flip-flop.

10. Design and implement a two bit digital comparator.

11. Design and implement Tri-state switch.

Laboratory Note Book — 2

Viva-voce — 3

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Set–2

Answer any *one* question (Lottery basis).

1. Design and implement a full adder circuit using NAND gates only.

2. Design and implement a two bit digital comparator.

3. Design and implement a half subtractor using NAND gates only.

4. Design and implement a 3×8 decoder.

5. Design and implement a 8 : 1 multiplexer.

6. Design and implement a 8 bit parity generator.

7. Design and implement a D flip-flop.

8. Design and implement a 4 bit synchronous counter.

9. Design and implement a JK flip-flop.

10. Design and implement a 4 bit adder using flip-flop.

11. Design and implement a master-slave JK flip-flop.

Laboratory Note Book — 2

Viva-voce — 3