2019

B. Sc.

1st Semester Examination

COMPUTER SCIENCE (Honours)

Paper : C 2-P

(Practical)

SET-I

Full Marks : 20 Time : 3 Hours

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Answer any one questions (Lottery basis). 1×15 =15

1. Design and implement a full adder circuit using NAND gates only.
2. Design and implement a two bit digital compatator.
3. Design and implement a 4bit synchronous counter.
4. Design and implement a 3× 8 decoder.

[Turn Over]

5. Design and implement a 4 bit adder using flip-flop.
6. Design and implement a JK flip-flop.
7. Design and implement a D-flip-flop.
8. Design and implement a Half subtractor using NAND gates only
9. Design and implement a 8 bit parity generator.
10. Design and implement a 8 : 1 multiptexer.

[PNB : 2 viva voce-3]

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1st Semester Examination

COMPUTER SCIENCE (Honours)

Paper : C 2-P

(Practical)

SET-II

Full Marks : 20 Time : 3 Hours

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Answer any one questions.

1. Design and implement a full adder circuit using NOR gates only.
2. Design and implement a full-subtractor using NAND gates only.
3. Design and implement a 8 : 1 Multiplexer.

[Turn Over]

4. Design and implement a two bit digital comparator.
5. Design and implement a 8 × 3 encoder.
6. Design and implement a D-flip-flop.
7. Design and implement a 8 bit parity generator.
8. Design and implement a JK master-slave flip flop.
9. Design and implement a 4 bit ripple ripple counter (up).
10. Design and implement a 4 it adder using flip-flop.

[PNB : 2 Viva-voce : 3]