UG/4th Sem/ELEC./H/19

2019

B.Sc. (Hons)

4th Semester Examination

ELECTRONICS

Paper - C9T

(Digital Electronics and Verilog/VHDL)

Full Marks : 40 Time : 2 Hours

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

1. Answer any *five* questions : 2×5=10

(i) Convert the following Hexadecimal number to Octal number

$(641A)_{16}$

(ii) Simplify the following :

$AB + \overline{A\bar{C}} + A\bar{B}C\,(AB + C)$

(iii) What is fan in and fan out ?

[Turn Over]

(iv) Why Multiplexer is called 'Universal Logic Module'?

(v) Write down two advantages of CMOS logic families.

(vi) How X-OR gate used as an inverter ?

(vii) Compare between combinational and sequential circuits.

(viii) What are the different 'types' used in VHDL?

2. Answer any *four* questions : 4×5=20

(i) Define the following terms related to digital ICs.

(a) Noise margin 1

(b) Propagation delay ^tPLH, ^tPHL 2

(c) Set up time 1

(d) Hold time. 1

(ii) Implement the function $F(A, B, C) = \Sigma m(1, 3, 5, 6)$ using decoder. What are the difference between demultiplexer and decoder. 3+2

(iii) What do you mean by 32K × 16 memory cell? How can you expand the memory capacity from (16 × 4) to (32 × 4). 1+4

(iv) What is race around condition ? How it can be overcome ? 5

(v) What is Totem-pole arrangement of a TTL NAND gate ? Briefly describe it by proper circuit diagram. 2+3

(vi) Briefly discuss about synthesis tools and Test benches of VHDL. 5

3. Answer any *one* question : 1×10=10

(i) (a) Implement the following function using 4 : 1 MUX only $f(A, B, C, D) = \Sigma(0, 2, 3, 5, 8, 9, 12, 14)$ 4

(b) Define register. 2

(c) What do you mean by structural modelling? 4

(ii) (a) Design a synchronous MOD 10 counter. 10

2019

B.Sc. (Hons)

4th Semester Examination

ELECTRONICS

Paper - C8T

(Operational Amplifiers and Applications)

Full Marks : 40 Time : 2 Hours

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

1. Answer any *five* questions : 2×5=10

(i) What is OPAMP ?

(ii) Explain the term input offset voltage in connection with an OP-AMP.

(iii) Draw the equivalent circuit of an OP-AMP.

(iv) What is gain-bandwidth product of an *OPAMP ?*

[Turn Over]

(v) Why does the voltage gain of OPAMP decrease at high frequencies ?

(vi) What is CMRR ?

(vii) What is slew rate of an OP-AMP ?

(viii) Write down the advantage of SMPS over ordinary power supply.

2. Answer any *four* questions : 4×5=20

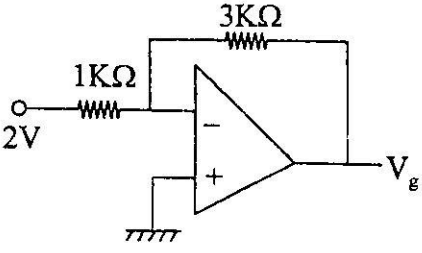
(i) Explain how an OPAMP can be used as an adder and a comparator. 2½+2½

(ii) State the characteristics of an ideal OP-AMP. 5

(iii) Draw a unity gain buffer and determine its input and output resistances. 2+1½+1½

(iv) Draw the ideal voltage transfer characteristics of an OP-AMP and also explain the same. 2+3

(v) For an inverting OP-AMP circuit (fig. below) determine input current and output voltage for an input-voltage of 2V. 5



(vi) Draw the circuit of voltage to current converter using OP-AMP and explain its operation. 2+3

3. Answer any *one* question : 1×10=10

(i) (a) Explain the working principle of a Schmitt Trigger using an OP-AMP.

(b) Draw the circuit diagram of an active lowpass 1st order Butterworth filter and describe its principle of operation.

5+(2+3)

(ii) (a) What is phase locked loop ?

[Turn Over]

(b) Draw the block diagram of a phase locked loop (PLL) and explain its principle of operation.

(c) Discuss how a PLL circuit can be used as a frequency multiplier. 2+4+4
