UG/4th Sem/Elec./19 (Pr.)

2019

B.Sc.

4th Semester Examination

ELECTRONICS (Honours)

Paper - C9P

(Digital Electronics and Verilog/VHDL Lab)

[Practical]

Full Marks : 20 Time : 3 Hours

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

Answer any *one* questions selecting it by a lucky draw.

1. Design and verify AND, OR, NOT and XOR gates using minimum number of NAND gates.

2. Convert the following Boolean expression into logic gate circuit and assemble it using logic gate IC's .

$$Y = (A+B)(\overline{A}+C)(B+D)$$

[Turn Over]

3. Design Half adder using basic and NAND gates and verify its truthtable.

4. Design Full adder using basic/NAND gate and verify its truth table.

5. Design Half subtrator using basic and NAND gates and verify is truth table.

6. Design Full Subtractor using basic / NAND gates and verify its truth table.

7. Design a seven segment display driver using 7447 IC.

8. Design a 4 : 1 MUX using NAND gates.

9. Construct RS, clocked RS and D flipflop using NAND gates and verify its operation.

10. Design 4 bit ripple counter using D/JK flipflop and verify its truth table.

11. Design four bit shift register using flipflop and basic gates. Study the following modes of operation

    (i) SISO

    (ii) SIPC

12. Write VHDL codes for full subtractor using basic and derived gates and verify its result.

13. Write VHDL codes for JK flipflop in behavioural modelling.

14. Write VHDL codes for 8 : 1 MUX.

15. Write VHDL codes for 4 bit binary adder.

16. Write VHDL codes for 3 bit binary to gray code converter using 3 : 8 decoder as a component.

17. Write a VHDL codes for 2 bit magnitude comparator.

18. Implement Half Adder and Full Adder circuit and verify its result.

19. Implement Half sub-tractor and Full-subtractor circuit and verify its result.

20. Design a 4×1 multiplexer using gates and verify its result.

21. Write VHDL code for 4×1 using logic gates and verify its result.

22. Write VHDL code for 3×8 decoder circuit and verify its result.

23. Write VHDL Code for Binaryb aray code converter and verify its result.

[Turn Over]

Distribution of Marks

Experiment	—	15
Laboratory Note Book	—	02
Viva-voce	—	03
Total		20