UG/5th Sem/Elec(H)/T/19

2019

B.Sc. (Honours)

5th Semester Examination

ELECTRONICS

Paper - C12T

(Theory)

(Microprocessor and Microcontrollers)

Full Marks : 40 Time : 2 Hours

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

1. Answer any *five* questions from the following : 2×5=10

   (i) What is a microprocessor ? How many bytes make a word of 32 bits ? 1+1

   (ii) The address capacity of 8085 μp is 64 kB. Explain. 2

   (iii) The memory address of the last location of an 8k byte memory chip is FFFFH. Find the starting address. 2

[Turn Over]

(iv) Explain machine cycle. 2

(v) How the vector address for a software interrupt is determined ? 2

(vi) What do you understand by Harvard architecture ? 2

(vii) Mention the features of microcontroller. 2

(viii) What is PIC 16F 887 ? 2

2. Answer any *four* questions from the following : 5×4=20

(i) Why do we need to demultiplex the bus AD_7-AD_0 ? Show a schematic diagram for this operation. 2½+2½

(ii) Compare between memory mapped I/O and I/O mapped I/O. 5

(iii) What do you understand by an Opcode fetch cycle ? List all ten control and status signals asserted by the 8085 microprocessor during the cycle. 2+3

(iv) Distinguish between the three modes of PPI 8255. 5

(v) What are the software instructions related to stack operations ? Exchange the contents of DE register pair with that of HL register pair, using PUSH and POP instructions. 2½+2½

(vi) Describe the memory organization of PIC 16F 877. 5

3. Answer any *one* question from the following : 10×1=10

(i) (a) Figure 1 shows the 74LS138 (3-to-8) decoder with three input signals : IO/$\overline{M}$, $\overline{RD}$ and $\overline{WR}$ from the 8085 μP. Specify and name the valid output signals.

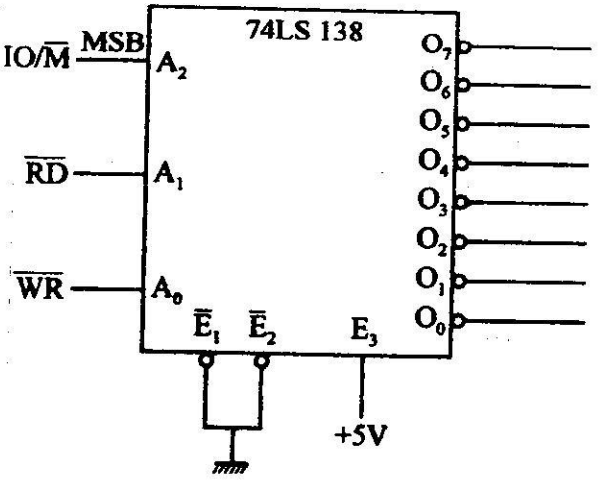

Figure - 1

[Turn Over]

(b) Calculate the delay in the following loop, assuming the system clock period is 0.5 μs: 4+6

Label	Mnemonics	8085 T-States
	LXI B, 12FFH	10
DELAY :	DCX B	6
	XTHL	16
	XTHL	16
	NOP	4
	NOP	4
	MOV A, C	4
	ORA B	4
	JNZ DELAY	10/7

(ii) Draw the architecture of PIC 16F 877 and describe it. 4+6