BCA/IS/DEL/1197/19 (Pr.)
(Set-1)

BCA 1st Semester Examination, 2019

DIGITAL ELECTRONICS LAB

(Practical)

PAPER – 1197

Full Marks : 100

Time : 3 hours

The figures in the right-hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

[SET-I]

Answer any **two** questions taking **one** from each Group (**Lottery basis**) : 30 × 2

GROUP – A

1. Design a Full Adder using NOR gates.

2. Implement basic gates using NOR gates.

3. Design a 8 : 1 MUX using minimum number of NAND gates and verify its truth table.

4. Implement Full Adder using 3 × 8 decoder and other necessary gates.

5. Implement the Boolean function using a MUX

$$F(A, B, C, D) = \sum(0, 1, 4, 7, 12, 13, 15)$$

6. Design a 3 to 8 line decoder using two 2 to 4 line decoder and other necessary gates.

7. Implement $Y = A'BC + AB' + B'C'$ using NAND gates only.

8. Design a circuit to convert Gray code to binary code.

9. Design a 1-bit comparator and verify its truth table.

10. Design a 2 to 4 line decoder using NAND gates only.

11. Design a half adder using NAND gates only and a full adder using two half adders.

12. Design a full subtractor using NOR gates only and verify its truth table.

13. Implement $z = \overline{x + y} + y + \overline{yz}$ using NAND gates only and verify its truth table.

14. Design a 4 bit 2's complement adder subtractor using 7483 or an equivalent and X-OR gates.

15. Implement the following Boolean function using a MUX :

$$F(W, X, Y, Z) = \sum(0, 1, 3, 4, 8, 9, 15)$$

GROUP – B

16. Construct clocked S-R flip-flop using NAND gates and verify its operation.

17. Design a T flip-flop using NAND and verify its output.

18. Convert a J-K F/F using D-F/F and verify its truth table.

19. Design a S-R F/F using J-K F/F and verify its truth table.

20. Design a 3-bit binary counter using J-K F/F.

21. Design a asynchronous down counter (MOD-6) using suitable gates.

22. Design a synchronous counter that counts 0,1, 3, 5, 7-9 using J-K F/F.

23. Design a Master-Slave JK flip-flop using NAND gates only and realize its characteristic table.

24. Design a 4-bit shift register using D F/F.

25. Design MOD-5 Synchronous Counter.

26. Design a 4 bit ripple counter using J-K flip-flop.

27. Design an asynchronous up counter (MOD 10).

28. Design a 4 bit bidirectional shift register using J-K flip-flop.

29. Design a 4 bit SISO register using D flip-flop and verify its truth table.

VIVA – 05

PNB – 05

[Internal Assessment – 30]

BCA/IS/DEL/1197/19(Pr.)
(Set-2)

BCA 1st Semester Examination, 2019

DIGITAL ELECTRONICS LAB

(Practical)

PAPER – 1197

Full Marks : 100

Time : 3 hours

The figures in the right hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

[SET–2]

Answer any **two** questions taking one from each Group (**Lottery Basis**) : 30 × 2

GROUP–A

1. Implement basic gates using NAND gates.

2. Design a Half-Subtractor using NAND gates.

3. Design a 3 × 8 decoder using two 2 × 4 decoder.

4. Design a 4 : 1 MUX using NAND gate only.

5. Design a circuit to convert binary to gray code.

6. Implement the boolean function using a MUX : $F(A, B, C, D) = \Sigma(0, 1, 2, 4, 5, 6, 7, 8, 9, 10, 15)$.

7. Design 8 : 1 MUX using two 4 : 1 MUX and other necessary gates.

8. Design a 1-bit comparator and verify its truth table.

9. Implement $Y = \Sigma(0, 1, 2, 8, 10, 11, 14, 15)$ using NAND gates only.

10. Design a circuit to convert gray to binary.

GROUP–B

11. Construct clocked J-K flip-flop using NAND gates and verify its truth table.

12. Design a *D* flip-flop using NAND gates and verify its truth table.

13. Design a MOD-5 asynchronous counter.

14. Design a MOD-6 synchronous counter.

15. Design a 4-bit SISO register using J-K flip-flop and verify its operation.

16. Design a 3-bit binary counter.

17. Design a synchronous counter to count

0-1-3-5-7-9-11

18. Design a 3-bit asynchronous down counter.

19. Design a 4-bit asynchronous up counter.

20. Design a MOD-8 synchronous counter.

Viva – 05 Marks

PNB – 05 Marks

Internal Assessment–30 Marks