2015

M.Sc.

4th Semester Examination

ELECTRONICS

PAPER—ELC-404

Full Marks : 50

Time : 2 hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

(VLSI Technology)

Answer *Q. No. 1* and any *three* from the rest.

1. (a) What is gettering ?

(b) How is a silicon dioxide layer grown for masking in VLSI technology ?

(c) Mention the advantages and disadvantages of electron beam lithography.

(d) What is CMOS latchup ?

(e) What do you understand by hard yield and soft yield ?

2×5

2. (a) Describe an ion implantation system with a schematic diagram.

(b) What are the problems entangles in ion implantation ? How can that be solved ?

(c) Mention SIMOX process and its uses.

3+(2+2)+(2+1)

3. (a) Describe electron cyclotron resonance (ECR) plasma etching with a schematic diagram of an ECR reactor.

(b) The electron densities in reactive ion etching (RIE) and hish-density plasma (HDP) systems range from 10^9 to 10^{10} cm^{-3} and 10^{11} to 10^{12} cm^{-3} respectively. Assuming the RIE chamber pressure is 200 mT and HDP chamber pressure is 5 mT. Calculate the ionization efficiency in RIE reactors and HDP reactors at room temperature.

(c) Explain the role of O_2 in plasma etching of Si in CF_4 + O_2 plasma.

4+(2+2)+2

4. (a) What are the different types of voltage break-down mechanism present in MOSFETs ?

(b) How does a LDD structure reduce short channel effects ?

(c) Explain a DMOS structure with a schematic disgram. Mention its merits and demerits.

2+3+(3+2)

5. (a) Draw a schematic diagram of a three phase CCD.

(b) Explain the operation of the CCD with potential energy and charge distribution of the device on the applications of clock pulses. Draw the clock wave forms and output signal.

(c) A three-phase n-type surface-channel CCD has the following specifications :

Electron density : $N_{max} = 2\times10^{12}$ cm^{-2}

Relative dielectric constant of the insulator : $\varepsilon_{ir} = 3{\cdot}9$

Insulator thickness : $d = 0{\cdot}15\ \mu m$

Insulator cross section : $A = 0{\cdot}5\times10^{-4}$ cm^2

Power dissipation allowable per bit : $P = 0{\cdot}67$ mW

(i) Determine the maximum stored charges per well.

(ii) Find the required applied gate voltage.

(iii) Choose the clock frequency.

$2+(3\frac{1}{2}+1\frac{1}{2})+(1+1+1)$

6. (a) What are the Moore's law and Rent's rule ?

(b) Estimate the number of gates that can be included on a logic-gate array chip which is to assembled in pin grid array package. Consider the Rent's exponent 0·5 and the average number of terminals required by a single logic block 4·5.

(c) Mention the different electrical performance criteria considered at the IC package. How is the most important practical electrical design problem in IC packages reduced ?

(2+2)+2+(2+2)

Internal Assessment — 10