2014

M.Sc.

3rd Semester Examination

ELECTRONICS

PAPER—ELC-301

Full Marks : 50

Time : 2 hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

(Microprocessor and its Applications)

Answer *Q. No. 1* and any *three* questions from the rest.

1. (a) Explain the physical address formation in 8086 μp.

   (b) Calculate analog voltages corresponding to the LSB and MSB for a 12-bit A/D converter calibrated for a 0 to 5V range. What is the percentage resolution of the converter?

   (c) What are the software instructions related to stack operations?

   (d) What is current loop interface?

(e) What are the major differences between 8086 μP and 8088 μP?

2×5

2. (a) Draw the architecture of 8085 μP. Compare the bus interface of 8085 μP with that of 8088 μP.

(b) The instruction code 0100 1111 (4FH) is stored in memory location 2005H. Illustrate the data flow when the instruction code is fetched by the MPU.

(5+2)+3

3. (a) Compare between memory-mapped I/O and peripheral I/O schemes. What do you understand by absolute and partial decoding?

b) Interface a 2kB memory chip to 8085 μp. Give the complete interfacing diagram. Use 3:8 decoder (74LS138) to decode the chip-select signal.

(4+2)+4

4. (a) An 8-bit binary number is stored in memory location XX50H. Write a program to :

I. (i) transfer the byte to the accumulator.

(ii) separate the two nibbles.

(iii) call the subroutine to convert each nibble into ASCII Hen code.

(iv) store the codes in memory locations XX60H and XX61H.

II. Write a subroutine to convert a binary digit into ASCII Hex code.

(b) Calculate the delay count that must be loaded the register C to obtain 1 ms delay between each count (use the clock frequency of the system = 2 MHz) :

Label	*Mnemomics*	*T-states*
	MVI B, 00H	7T
NEXT :	DCR B	4T
	MVI C, COUNT	7T
DELAY :	DCR C	4T
	JNZ DELAY	10/7T
	MOV A, B	4T
	OUT PORT#	10T
	JMP NEXT	10T

(3+3)+4

5. (a) Explain the Read/Write control logic and the registers of the IC 8251A.

(b) Draw the data loading sequence and describe it for the IC 8251A.

$5+(2\frac{1}{2}+2\frac{1}{2})$

6. (a) Compare synchronous and asynchronous serial transmission modes. How the error checks are made in data communication?

   (b) Draw the RS 232C equivalent circuit model and specify the various parameters of the interface specification.

$(2+3)+(2\frac{1}{2}+2\frac{1}{2})$

[Internal Assessment — 10]