2014

M.Sc.

4th Semester Examination

ELECTRONICS

PAPER—ELC-404

Full Marks : 50

Time : 2 hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

(VLSI Technology)

Answer *Q. No. 1* and any *three* from the rest.

1. (a) What is extrinsic diffusion ?

(b) Why NMOS are preferred to PMOS in VLSI technology ?

(c) Mention the merits of utilizing BiCOMs technology in VLSI.

(d) What do you understand by the functional yield and parametric yield ?

(e) Draw a cross-sectional view of a buried-channel CCD. 2×5

2. (a) Describe with a diagram the various charges associated with thermally oxidized silicon.

   (b) What is the bird's beak structure in the oxidation process ? How is it prevented ?

   (c) If a silicon oxide of thickness x is grown by thermal oxidation, what is the thickness of silicon being consumed ? The molecular weight of Si is 28.9 g mol^{-1}, and the density of Si is 2.33 g cm^{-3}. The corresponding values for SiO_2 are 60.08 g mol^{-1} and 2.21 g cm^{-3}.

   4+(2+1)+3

3. (a) What are the different lithographic technologies used in VLSI ? Make comparisons among them.

   (b) Which type of resist is a better one : a positive resist or a negative resist ? Give reasons.

   (c) What is chemical-amplified resist ?

   (1+5)+2+2

4. (a) Explain the circuit shown in Fig. 1 and draw its stick diagram :

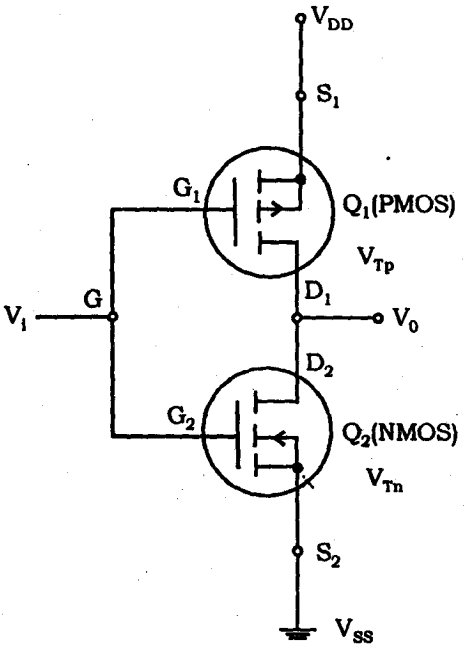

Fig. 1

(b) Describe the steps involved to fabricate a monolithic integrated circuit of the electrical circuit shown in Fig. 1.

(2+2)+6

5. (a) Why do we scale MOS transistors ? Compare between constant voltage scaling and constant electric field scaling.

   (b) A microprocessor was fabricated in a 0.25 μm technology and was able to operate at 100 MHz, consuming 10W using a 2.5V power supply.

   Using fixed voltage scaling, what will the speed and power consumption of the same processor be if scaled to 0.1 μm technology ?

   (c) How does the short channel effect reduce in a recessed-channel MOSFET ?

(3+2)+2+3

6. (a) What are the different chip-to-package inter-connections used in VLSI ? Compare the different attachment methodologies.

   (b) Draw the assembly flow chart for packages using wire.

   (c) Explain the power limitation effect on IC packaging.

(1+4)+3+2

Internal Assessment — 10