PG/IIIS/ELC-301/13

M.Sc. 3rd Semester Examination, 2013

ELECTRONICS

(*Microprocessor and its Applications*)

[Theory]

PAPER –ELC-301

Full Marks : 50

Time : 2 hours

Answer **Q. No. 1** and any **three** questions from the rest

The figures in the right-hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

1. Answer *all* questions : 2 × 5

(*a*) The memory address of the last location of an 8 K byte memory chip is FFFFH. Find the starting address.

(*b*) List the sequence of events that occurs when the 8085 μp reads from memory.

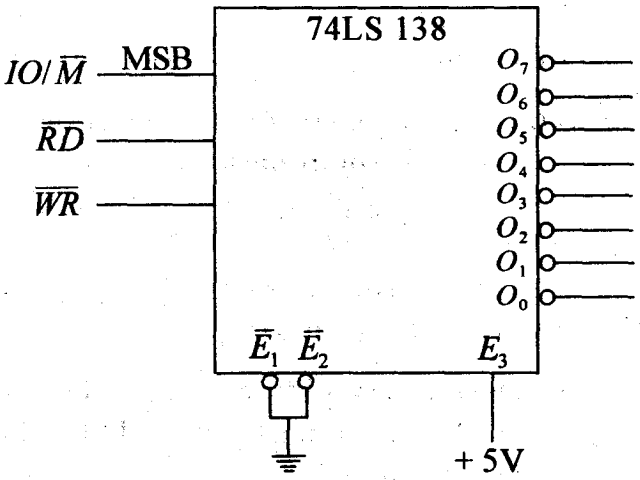
(*c*) Explain the instruction XTHL.

(*d*) How does the microprocessor differentiate among a positive number, a negative number and a bit pattern ?

(*e*) How the chip 8251 is programmed ?

2. (*a*) Why do we need to demultiplex the bus AD_7-AD_0 ? Explain with a schematic to demultiplex the bus.

(*b*)



(*Continued*)

The above figure shows 74LS138 (3-to-8) decoder with the three input signals :

$IO/\overline{M}$, $\overline{RD}$ and $\overline{WR}$ from the 8085 μp. Specify the name the valid output signals. (2 + 5) + 3

3. (*a*) Write down the distinguishing features between memory mapped I/O scheme and I/O mapped I/O scheme. If high-order lines are partially decoded, how can one determine whether it is peripheral I/O or memory-mapped I/O ?

(*b*) 2 KB RAM, 2 KB ROM, one input and one output device are to be interfaced with 8085 μp. Employ memory mapped I/O scheme to execute the above. (4 + 2) + 4

4. (*a*) Compare instructions CALL and RET to the instructions PUSH and POP. Exchange the contents of DE register pair with that of HL register pair, using PUSH, POP instructions.

(*b*) The following program has a delay subroutine located at location 2060H. Read the program and answer the questions given at the end of the program.

Memory location (H)	Mnemonics	
2000	LXI SP, 20CD H	; Main Program
2003	LXI H, 0008 H	
2006	MVI B, OF H	
2008	CALL 2060 H	
200 B	OUT 01 H	
↓	DCR B	
	↓	
↓	CONT D	
2060	PUSH H	; Delay Subroutine
2061	PUSH B	
↓	MVI B, 05 H	
↓	LXI H, COUNT	
	↓	
↓	POP B	
↓	POP H	
↓	RET	

(*Continued*)

(*i*) When the execution of the CALL instruction located at 2008 H-200 A H is completed, list the contents stored at 20 CC H and 20 CB H, the contents of the program counter and the contents of the stack pointer register.

(*ii*) List the stack locations and their contents after the execution of the instructions PUSH H and PUSH B in the subroutine.

(*iii*) List the contents of the stack pointer register after the execution of the instruction PUSH B located at 2061 H.

(*iv*) List the contents of the stack pointer register after the execution of the instruction RET in the subroutine.

$(3+2)+\left(2+2+\frac{1}{2}+\frac{1}{2}\right)$

5. (*a*) Draw the functional block diagram of PIC 8259 and describe how the chip responds to interrupts.

(*b*) Explain the interrupt process in fully nested mode. (3 + 3) + 4

6. (*a*) Draw a schematic diagram of a DTE-DCE interface in a communication environment. Explain the general transmission/reception format for asynchronous communication.

(*b*) Why modems are used in case of digital transmission of data ? (3 + 4) + 3

[*Internal Assessment* : 10 Marks]