PG/IVS/ELC-405/13(Pr.)

M.Sc. 4th Semester Examination, 2013

ELECTRONICS

(*Advanced Electronics Lab*)

(Practical)

PAPER – ELC - 405

Full Marks : 50

Time : 3 hours

Answer any **one** question selecting it by a lucky draw

In each of the following questions, you have to save the design file by "your roll no., –design" and then save the plot in a file "your roll no., –plot".

1. Design a first order low pass active filter with cut-off frequency 1kHz in PSPICE. Simulate the circuit and plot the gain versus frequency curve. Also verify the cut-off frequency from the plot with its given value.

2. Design a non-inverting amplifier circuit using OP-AMP taking input resistor R_1 = 1 kΩ, feed-back resistor R_2 = 6.8 kΩ and load resistor R_3 = 10 kΩ. Apply sine wave as an input signal with suitable amplitude and frequency of your choice. Simulate the circuit using PSPICE and plot the input voltage V_{in} versus time and output voltage V_o versus time in same graph. Also verify the gain of the amplifier with given value.

3. Design a second order active high pass Butter worth filter with cut-off frequency 3 kHz. Simulate the circuit using PSPICE and plot the gain versus frequency curve. Also verify the cut -off frequency with the given value.

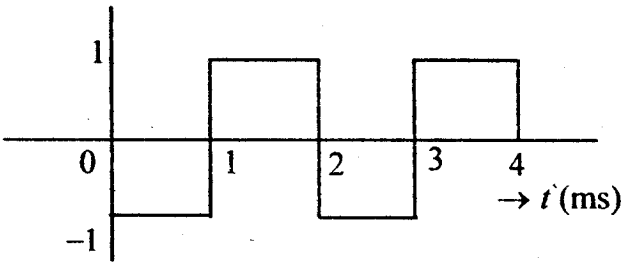
4. Design an astable multivibrator circuit with frequency 3 kHz and duty cycle 50 % using IC 555. Simulate the circuit using PSPICE and plot the output versus time curve. Also verify the output frequency and duty cycle of the plot with the given value.

5. Design an inverting amplifier circuit using OP-AMP taking input resistor R_1 = 1 kΩ, feedback resistor R_2 = 10 kΩ and load resistor R_3 = 10 kΩ. Apply sine wave as an input signal with suitable amplitude and frequency of your choice. Simulate the circuit using PSPICE and plot the input voltage V_{in} versus time and output voltage V_o versus time in the same graph. Also verify the gain of the amplifier with the given value.

6. Design a second order active low pass Butterworth filter with cut off frequency 1 kHz. Simulate the circuit using PSPICE and plot the gain versus frequency curve. Also verify the cut -off frequency with the given value.

7. Design a first order high pass active filter with cut-off frequency 3 kHz in PSPICE. Simulate the circuit and plot the gain versus frequency curve. Also verify the cut-off frequency of the plot with its given value.

8. Design an integrator circuit using op-amp taking input resistance $R_1 = 1\ k\Omega$, feed back resistance $R_1 = 6{\cdot}8\ k\Omega$ feedback capacitance $C_2 = 0.1\ \mu F$ and load resistance $R_3 = 10\ k\Omega$. Simulate the circuit using PSPICE and plot the transient response of the output voltage for a duration of 0 to 4 ms in steps of 50 μs for the input existation given below.



9. Design a second order active high pass Butterworth filter with cut off frequency 5 kHz. Simulate the circuit using PSPICE and plot the gain versus frequency curve. Also verify the cut-off frequency with the gain value.

10. Design a 3 bit synchronous odd counter using JK flip-flop. Verify the count sequence by LED display.

11. Design a M OD5 synchronous up counter using JK flip-flop. Verify the count sequence by LED display.

12. Design a 3 bit synchronous even counter using JK flip-flop. Verify the count sequence by LED display.

Marks distribution(for PSPICE)

For Question No. 1 to 9

Theory	:	07
Circuit Design	:	10
Simulation	:	10
Verification & Accuracy	:	05
Discussion	:	03
Viva	:	10
Laboratory Note Book	:	05
Total	:	50 Marks.

Marks distribution(for Digital)

For Question No. 10 to 12

Theory	:	05
Circuit Design	:	15
Implementation	:	07
Experimental Result	:	05
Discussion	:	03
Viva	:	10
Laboratory Note Book	:	05
Total	:	50 Marks.