PG/IVS/ELC-404/13

M.Sc. 4th Semester Examination, 2013

ELECTRONICS

(*VLSI Technology*)

(Theory)

PAPER—ELC - 404

Full Marks : 50

Time : 2 hours

Answer **Q. No. 1** and any **three** from the rest

The figures in the right-hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

1. Answer *all* questions : 2 × 5

(*a*) What do you understand by 'a class 100 clean room' ?

(*b*) How can you grow a thin oxide layer ?

(*c*) Why do you require a twin-tub process in a CMOS fabrication ?

(*d*) What is a stick diagram ? Draw a monochrome stick diagram of a CMOS inverter.

(*e*) What is the most important practical electrical design problem in IC packages ? How is the problem reduces ?

2. (*a*) Explain the two-step diffusion process which is commonly used in integrated circuit processing.

(*b*) What do you mean by the intrinsic diffusivity and extrinsic diffusivity ?

(*c*) For a boron diffusion in silicon at 1000°C, the surface concentration is maintained at 10^{19} cm^{-3} and the diffusion time is 1 hour. Find the location where the dopant concentration reaches 10^{15} cm^{-3}. Given the diffusion coefficient of boron at 1000°C is 2×10^{14} cm^2s^{-1}. 3 + (2 + 2) + 3

3. (*a*) Mention the features that must be considered in metallization scheme in VLSI. Enumerate the methods of depositing metal films in VLSI.

   (*b*) Explain the problems arising from aluminium deposition. How can these problems be minimized? (2 + 2) + (3 + 3)

4. (*a*) Discuss with diagrams the steps followed in the fabrication of an *n*-channel enhancement mode MOSFET.

   (*b*) Explain the short-channel and narrow channel effects. 6 + (2 + 2)

5. (*a*) Draw the schematic diagram of a three-phase CCD with overlapping gate electrodes. Explain its operation with potential energy and charge distributions.

   (*b*) Draw a cross-sectional view of a buried channel CCD (BCCD). Explain the importance of BCCD. (3 + 4) + (2 + 1)

6. (*a*) What do you mean by IC packaging? Discuss the chip-to-package interconnection techniques used in VLSI.

(*b*) Find the number of gates that can be included on a logic-gate-array chip which is to be assembled in a 100 I/O package. Assume the average number of terminals required by a single logic block is 4·5 and the Rent's exponent is 0·5. (2 + 6) + 2

[*Internal Assessment* : 10 Marks]