M.Sc.

2011

4th Semester Examination

ELECTRONICS

PAPER—EL-2204

Full Marks : 40

Time : 2 Hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer *Q. No. 1* and any *three* from the rest.

1. Answer any *five* questions : 2×5

(a) What do you mean by the λ-based design rules for the layout of VLSI circuits?

(b) Why is silane more often used for poly-silicon deposition than silicon chloride?

(c) Mention the features that must be considered for metallization in VLSI.

(d) Why do you require a twin-tub process in a CMOS fabrication?

(e) What is the most important practical electrical design problem in IC packages? How is the problem reduced?

(f) State the merits and demerits of contact printing method.

2. (a) Describe with a schematic diagram an ion implantation system.

   (b) What are the problems involved in an ion implantation? How can they be solved? 5+(3+2)

3. (a) Explain different methods of etching in VLSI technology.

   (b) How can SiO_2 layers, and Al and Al-alloy films be etched out?

   (c) The electron densities in a reactive ion etching (RIE) system and high-density plasma (HDP) system range from $10^9 - 10^{10}$ and $10^{11} - 10^{12}$ cm^{-3}, respectively. Assuming the RIE chamber pressure is 200m Torr and HDP chamber pressure is 5m Torr, calculate the ionization efficiency in RIE reactors and HDP reactors at room temperature.

   $4+(1\frac{1}{2}+1\frac{1}{2})+3$

4. (a) Discuss the diagrams the steps followed in the fabrication of an n-channel depletion MOSFET.

   (b) How is the threshold voltage of a MOSFET controlled?

   (c) Compare among bipolar, CMOS and BiCMOS technologies. 5+2+3

5. (a) Draw the schematic diagram of a three-phase CCD with overlapping electrodes. Explain its operation with potential wells and change distribution.

   (b) Discuss the importance of the buried channel CCD. (3+5)+2

6. (a) What are the criteria to be fulfilled for a good package design in VLSI technology?

   (b) Explain different chip-to-package interconnection techniques used in VLSI.

   (c) What do you mean by the functional yield and parametic yield? $2+5+(1\frac{1}{2}+1\frac{1}{2})$
