PG/IVS/EL-2204/10

M.Sc. 4th Semester Examination, 2010

ELECTRONICS

(VLSI Technology)

PAPER—EL-2204

(Theory)

Full Marks : 40

Time : 2 hours

Answer **Q. No. 1** and any **three** from the rest

The figures in the right-hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

1. Answer any *five* questions : 2×5

(*a*) Give reasons to determine which environment you consider the best : a class 10, a class 100, or a class 1000.

(*b*) Why is 'ion chanelling' not a favoured situation in the implantation of atoms in a semiconductor ?

(*c*) How can you grow a silicon nitride thin film ? Mention its uses in VLSI fabrications.

(*d*) What is the bird's beak structure ? How is it prevented ?

(*e*) What are the factors that restrict an arbitary scaling down of the MOSFET gate oxide thickness ?

(*f*) Mention the factors to be considered for packaging a VLSI chip.

2. (*a*) What do you mean by predeposition and drive-in diffusions ?

(*b*) Establish Fick's diffusion equation. How does the diffusivity vary with the temperature and dopant concentration ?

(*c*) For a boron diffusion in silicon at 1000°C, the surface concentration is maintained at 10^{19} cm^{-3} and diffusion time is 1 hour. Find the total number of dopant atoms per unit area of the semiconductor, and the junction depth

where the dopant concentration reaches 10^{15} cm^{-3}. Given diffusion coefficient of boron in silicon at 1000°C is 2×10^{14} $cm^2 s^{-1}$.

2 + (2 + 2) + (2 + 2)

3. (*a*) What are the different methods used for producing the image of a mask on a wafer surface ? Discuss the methods.

(*b*) What are the photoresist and electron resist ? Which type of resist is a better one : a positive resist or a negative resist ? Give reasons.

(1 + 5) + (2 + 2)

4. (*a*) Describe, with neat diagrams, the fabrication steps for a CMOS.

(*b*) What is the utility of a refilled trench technique in the fabrication of a CMOS device ? 8 + 2

5. (*a*) Compare among bipolar, CMOS and BiCMOS technologies.

(*b*) What is meant by "VLSI design rules" ?

(*c*) What is a stick diagram ? Draw stick diagrams of a PMOS, an NMOS and a CMOS inverter. $3 + 2 + (2 + 1 \times 3)$

6. Write notes on any *two* : 5×2

(*i*) Etching

(*ii*) Hot electron effects in VLSI structures

(*iii*) Electromigration.