2009

M.Sc.

2nd Semester Examination

ELECTRONICS

PAPER—EL-1202

Full Marks : 40

Time : 2 Hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer *Q. No. 1* and any *three* from the rest.

1. Answer any *five* questions : 2×5

(a) Prove that $A \oplus B \oplus \overline{C} = \overline{A \oplus B \oplus C}$.

(b) What is the major advantage and disadvantage of flash ADC ?

(c) Derive the characteristic equation of a D flip-flop from the characteristic equation of a JK flip-flop.

(d) Define the Fan-out of a logic gate.

(e) Which input of a commercially available decoder IC chip can be utilised to use the decoder as a demultiplexer ?

(f) What do you mean by Figure of Merit of a digital IC ?

(g) Which theorem has been utilised for developing the method of minimisation of Boolean function using K-map ?

(h) Write down the function of chip select and Read/Write input of a memory chip.

2. (a) How an 8–to–1 MUX can be designed using all 4–to–1 MUXs ? (No other logic can be used). Draw the circuit and explain the operation.

   (b) How a 4–to–1 MUX can be converted to a 2–to–1 MUX ? 6+4

3. Using a 4–to–16 decoder design a circuit with following feature :

   "Circuit should produce logic-1 output when the 4-bit binary input to the decoder is divisible by 3 but greater than 5. 10

4. (a) Find out the minimal expression of the given function :

   $$F = \Sigma m(3, 4, 5, 7, 9, 13, 14, 15)$$

   And draw the minimal circuit using NOR gates only.

   (b) Design a full adder circuit using a single decoder with active-low outputs and NAND gates. (4+3)+3

5. (a) Give the construction of a 555 timer IC.

   (b) Explain how the timer is used as a monostable multivibrator.

   (c) Design a circuit using 555 IC to generate of 5 KHz frequency and duty cycle 60%. 3+4+3

6. (a) Describe the relative advantages of MOS circuits as compare with BJT circuits.

   (b) Draw the circuit diagram for DRAM cell and explain its read and write operation.

   (c) Construct a CMOS circuit to implement the following Boolean function :

   $$F = (A + B + C)\, D.$$ 1+5+4

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