2012

MCA

1st Semester Examination

BASIC ELECTRONICS & DIGITAL LOGIC

PAPER—MCA-103

Full Marks : 100

Time : 3 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer any *seven* questions.

1. (a) What are intrinsic and extrinsic semiconductors? What are p-type and n-type crystals? Is an n-type semiconductor negatively charged? 2+2+1

(b) What is static resistance & what is dynamic resistance? 2

(c) Draw the practical volt-ampere characteristics of Ge-diodes and Si-diodes showing the cut in voltages. 3

2. (a) Establish the relation $I_c = \beta I_B + (1+\beta) I_{CBO}$ for CE configuration in active region. 2

(b) A transistor with $\alpha = 0.98$ is operated in CB configuraton. If the emitter current is 3 mA and the reverse saturation current is $I_{CO} = 10\mu A$, what are the base current and the collector current? 3

(c) Draw the output characteristic curves of an n-p-n transistor in CE mode. Discuss about the different operating regions. 5

3. (a) What is Thermal runaway? 2

(b) Define JFET parameters and give the relation between them. 5

(c) Write the difference between FET and BJT. 3

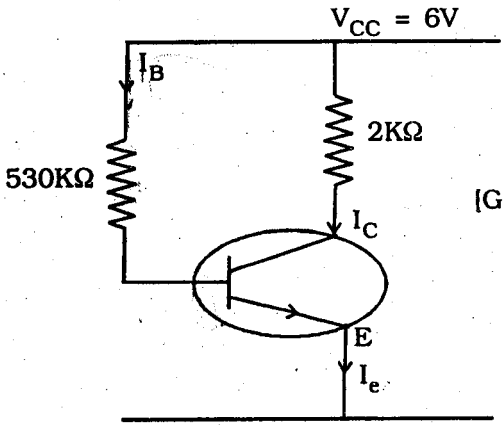
4. (a) What is OP-AMP? Define CMRR & slew rate. 1+2+2

(b) Derive the expression for the OPAMP used as an adder and draw the circuit diagram. 3+2

5. (a) What do you mean by faithful amplification? 2

(b) Draw and briefly explain the circuit diagram of an emitter bias. 4

(c) The circuit of a base resistor biased transistor is given below : 5



[Given β = 100]

(i) Draw the DC load line. 2

(ii) Calculate the operating point. 2

6. (a) Simplify Boolean function xz + x'yz to a minimum number of literals. 2

(b) Use only NOR gates to design a clocked S–R flip-flop. What is forbidden state ? 4+2

(c) Show that the dual of the exclusive – OR is equal to its complement. 2

7. (a) Design full subtractor using 4 : 1 Multiplexer. 5

   (b) Write short notes on Octal to binary encoder. 3

   (c) What is parity bit generator? 2

8. (a) Draw and explain working principle of clocked master-slave JK flip-flop using NAND gates only. 4

   (b) What is the basic difference between a D flip-flop and a T flip-flop? 2

   (c) Use only NAND gates to design a clocked S–R flip-flop and show its truth table. 4

9. (a) What is universal shift register? Design it. 6

   (b) What are the advantages and disadvantages of ripple counter? 2

   (c) What is the modulus of a counter? 2

10. (a) Design 3 bit synchronous down counter. 5

    (b) Design XOR gate using NAND gates. 2

    (c) What is the difference between EPROM and EAROM? 3

[Internal Assessment — 30]