MCA 2nd Semester Examination, 2012

COMPUTER ARCHITECTURE AND ORGANIZATION

PAPER – CS-MCA-203

Full Marks : 100

Time : 3 hours

Answer **Q.No.1** and any **five** from the rest

The figures in the right hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

1. Answer any *five* questions : 2 × 5

(*a*) Give two reasons why a RISC processor is better than a CISC processor.

(*b*) What do you mean by associative ~~memory~~ mapping ?

(*c*) List two differences between DRAM and SRAM.

(*d*) Show that adding B after the operation $A + \overline{B} + 1$ restores the original value of A. What happens to end carry ?

(*e*) Differentiate between Direct and Indirect addressing mode.

(*f*) What do you mean by Machine cycle and Instruction cycle ?

2. (*a*) What do you mean by stack organisation ? With the help of diagram explain memory stack organization.

(*b*) What is the difference between a volatile and destructive read out memory ? Are destructive read out memories necessarily volatile. (2 + 6) + (2 + 2)

3. (*a*) What is the difference between floating point and fixed point number formats ? Explain the floating point format briefly with the help of an example. What is the precision w.r.+ floating point number ?

(*b*) What is interrupt ? Briefly explain the any three interrupt conditions. (3 + 4 + 1) + (1 + 3)

4. (*a*) A processor have 16 address line and 8 data lines. It has also $\overline{RD}$, $\overline{WR}$ control lines other than power line. Give the schematic diagram showing how you can interface two 8K ROM and two 8K RAM chips with the processor. Mention the address space occupied by the chip.

   (*b*) What do you mean by mapping on to cache lines ? Explain briefly set associative mapping. What are the advantages and disadvantages of associative mapping over set associative mapping ? (4 + 2) + (2 + 2 + 2)

5. (*a*) Illustrate the algorithm for multiplication of signed 2's complement number.

   (*b*) Show the steps involved, while multiplying two binary number 11111 (multiplicand) and 10101 (multiplier) is above defined algorithm.

   (*c*) Write a program to evaluate the arithmetic statement :

$$X = \frac{A - B + C * (D * E - F)}{G + 4 * K}$$

   (*i*) Using a general register computer with three address instruction.

(*ii*) Using a stack organized computer with zero-address operation instructions. 4 + 4 + 4

6. (*a*) What is cache memory ? Why is it needed ? Explain the term-principle of locality, valid bit and dirty bit, cache lines or block.

(*b*) A digital computer has a common bus system for 16 registers with 32 bits in each. The bus is constructed with multiplexer.

(*i*) How many selection inputs are there in each multiplexer

(*ii*) What size of multiplexer are needed

(*iii*) How many multiplexers are needed

(*iv*) Design the bus system.

(2 + 2 + 3) + (1 + 1 + 1 + 2)

7. (*a*) An 8-bit computer has a register *R*. Determine the values of status bits *C* ,*S*, *Z* and *V* after each of the following instructions. The initial value of register *R* in each case is hexadecimal 72. The number below are also in hexadecimal.

(*i*) Add immediate operand C6 to R

(*ii*) AND immediate operand 8D to R.

(*iii*) Exclusive - OR R with R

(*b*) Give block diagram of DMA controller. How does the CPU initialize the DMA transfer ?

(2 + 2 + 2) + (3 + 3)

8. (*a*) A computer memory has 8M words with 32 bits per word. How many bits are needed is MAR if all the words are to be addressed ? How many bits are needed for MBR ? How many binary storage cells are needed ?

(*b*) Design a bus system in a multi-registering configuration for 8, 16 bit registers. Explain the process applied. (2 + 2 + 2) + 6

[*Internal Assessment* – 30 Marks]