2015

M.Sc.

1st Semester Examination

COMPUTER SCIENCE

PAPER—COS-102

Full Marks : 50

Time : 2 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer any *four* questions.

1. Consider the following reservation table of a four stage pipeline processor.

	1	2	3	4	5	6	7
S_1	X					X	
S_2			X				X
S_3		X		X			
S_4			X		X		

(a) Find out collision vector.

(b) Draw state diagram.

(c) List all simple and greedy cycles.

(d) Calculate MAL. 2+4+3+1

2. (a) Draw and explain UMA Model of multiprocessor.

(b) Discuss Snoopy protocal of multiprocessor.

(c) Compare the loosely coupled & tightly coupled multiprocessor system.

3. (a) Explain the inclusion and coherence properties of memory.

(b) Compare the different types of locality of reference.

(c) A 3 level memory system having cache access time of 15 ns and disk access time of 80ns has a cache hit ratio of 0·96 and main memory hit ratio of 0·9. What should be the main memory access time to achieve effective access time of 25 ns.

3+3+4

4. (a) What is instruction pipelining?

(b) What is pipeline hazards? What are the different types of hazards in instruction pipelining?

(c) Explain different classes of data hazards.

2+(1+2)+5

5. (a) Explain Flynn's classification of computer with proper diagrams.

(b) Consider the execution of a program of 20,000 instructions by on linear 5 stage pipeline processor with a clock rate, 40MHz where me instruction is issued per clock cycles. Calculate the speedup of the pipeline over its equivalent non-pipeline processor, the efficiency and through put.

5+(2+1+2)

6. (a) What is virtual memory ?

(b) What is the difference between RISC & CISC ?

(c) Suppose there is a system with 256MB main memory space of the processor is 256 MB. The block size is 128 bytes. There are 8 blocks in a cache set. Determine size of the sub-fields (inbits) in the address for associate, direct and set associative mapping cache schemes.

[Internal Assessment — 10 Marks]