2015

M.Sc.

1st Semester Examination

COMPUTER SCIENCE

PAPER—COS-102

Full Marks : 50

Time : 2 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer any *four* questions.

1. (a) Describe the architecture of a typical super scalar VLIW processor with the help of block diagram.

(b) What is multiprocessor cache coherence problem and what are resolution techniques.

6+4

2. Suppose we want to design a pipelined adder (32 bit, 8 stages) with basic ripple carry adders. Suppose a full adder delay is 1ns and clock skew is 10%, set time is 0.1s. What kind of pipelining is suitable for this and why ?

10

3. (a) Explain loosely coupled and tightly coupled multiprocessor system. Compare them. 8

   (b) Distinguish between UMA and NUMA architecture models. 2

4. (a) Define Amdahl's law of speed up performance.

   (b) Differential multiprocessor and multicomputers.

   (c) Define Flynn's classification.

   3+3+4

5. (a) What is array processor ? State different types of array processor with proper diagram. 4

   (b) Difference between array and vector processing. 2

   (c) Classify the parallel processor system according to the Flynn's 4

6. (a) What is vector processing ? State suitable architecture of vector processing. 4

   (b) State different conflicts of instruction pipe line. 3

   (c) State set-associate mapping technique of catche. 3

[Internal Assessment — 10 Marks]

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