2019

MCA

Computer Science

2nd Semester Examination

PAPER – 202

Full Marks : 100

Time : 3 Hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their

Own words as Far as practicable.

Illustrate the answers wherever necessary.

Answer Q. No. 1 and any ***FIVE*** from the rest.

1. Answer any ***FIVE*** questions : 5x2=10

a) Compare between arithmetic and logical operation.

b) What is an opcode ? How many bits are needed to specify 32 distinct operations ?

c) What are the components of i/o interface ?

d) What are the 2 ways to detect overflow in an n-bit adder ?

e) Define pipeline processing .

f) Briefly explain the floating point representation with an example .

g) What is write-through protocol ?

2. a) A digital computer has a common bus system for 16 registers of 32 bits each .

The bus is constructed with multiplexers .

i) How many selection inputs are there in each multiplexer ?

ii) What size of multiplexers is needed ?

iii) How many multiplexers are there in the bus ?

b) State the differences between cache memory and virtual memory .

c) What is strobe signal ? 6+4+2

3. a) Explain the Booth's algorithm for multiplication of signed two's complement numbers.

   b) What are the Characteristics of SRAMs and DRAMs ? 8+4

4. a) Compare the hardwired control with micro programmed control in terms of complexity of the instruction set, ease of modification and clock speed with a neat block diagram.

   b) Explain how the basic computer registers are connected to the common bus ? (6+6)

5. a) What is direct memory access (DMA) ? Why are the read and write control lines in a DMA controller bi directional ?

   b) What is the difference between isolated I/O and memory mapped I/O ?

   c) What are the basic differences between branch instruction, a call subroutine instruction and program interrupt ? 4+4+4

6. a) Design the hardware of addition and subtraction of fixed point signed magnitude numbers.

   b) Explain priority interrupt in detail . 7+5

7. a) What is asynchronous data transfer ? Explain in detail .

   b) How many 128x8 RAM chips are needed to provide a memory capacity of 2048 bytes ?

c) How many lines of the address bus must be used to access 2048 bytes of memory ? how many of these lines will be common to all chips ?

d) How many lines must be decoded for chip select ? Specify the size of the decoders .

(3+3+3+3)

8. Write short note on : (any three) 3x4

a) Direct Mapping

b) Memory Hierarchy

c) Timing Diagram

d) Instruction Cycle

e) Control Word

[INTERNAL ASSESSMENT : 30 Marks]