2019

MSc

2nd Semester Examination

ELECTRONICS

PAPER – ELC-203

Full Marks: 50

Time: 2 Hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their

Own words as far as practicable.

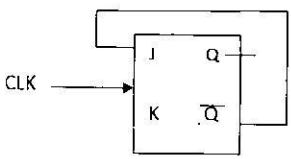
Illustrate the answers wherever necessary.

1. Answer any ***04*** questions out of ***08*** Questions. 2×4

i) Why is ECL called the fastest of all logic families?

ii) Implement the following function with a MUX: F(a, b, c) = Σm (1, 3, 5, 6) choose a and b as select inputs.

iii) The J-K FF shown below is initially cleared and then clocked for 5 pulses, the sequence at the Q output will be.



(A) 010000
(B) 011001
(C) 010010
(D) 010101

iv) Implement the logic expression Y = AB(C+DE) using CMOS logic.

v) Find out the output voltage when input is 0100 using 4 bit R – 2R ladder type ADC.

vi) Differentiate between static and dynamic memory.

vii) A binary channel with bit rate r_b = 36000 bits per second (b/s) is available for PCM voice transmission.Evaluate the approximate values of the sampling rate fs, the quantizing level q and the number q binary digits v. Assume fm = 3.2 kHz.

viii) Write down advantages of PCM system over other communication system.

2. Answer any ***04*** questions out of ***08*** questions. 4×4

i) Write short note on successive approximation type A/D converter.

ii) Design Ring counter, mention its different states.

iii) Convert SR to JK F/F.

iv) Design 2 – bit magnitude componator.

v) Design of a 4 bit Binary to gray code converter.

vi) Reduce using mapping the expression $f = \Sigma m (0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$ and implement the real minimal expression in universal logic.

vii) A television signal having a bandwidth of 4.2 MHz is transmitted using binary PCM system. Given that the number of quantization level is 512. Determine.

1) Code word length 2) Transmission bound width 3) Final bit rate

4) Output signal to quantization noise ratio.

viii) With the help of block diagram describe PCM generator.

3. Answer any ***02*** questions out of ***04*** questions. 2×8

i) Design of a synchronous BCD counter using J – K Flip – flops.

ii) With the help of proper circuit diagram explain the operation of monostable multivibrator.

iii) Explain the operation of two input TTL NAND gate.

iv) a) Design a combinational circuit that accepts a 3 – bit number as input and generates an output binary number equal to the sequence of the input number using ROM.

b) Write short notes on change – coupled device.

(Internal assessment - 10 marks)