PG/IIIS/ELC-303/19

M.Sc. 3rd Semester Examination, 2019

ELECTRONICS

(*VLSI Engineering*)

PAPER –ELC-303

Full Marks : 50

Time : 2 hours

Answer **all** questions

The figures in the right-hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

1. Answer any *four* questions : 2 × 4

(*a*) What is Moor's law ?

(*b*) Compare the transform characteristics of *n*-channel and *p*-channel MOSFETs.

(*c*) Why do we scale MOS transistor ?

(*d*) Mention basic steps in IC fabrication.

(*e*) What are the precautions to be taken for IC packaging ?

(*f*) What do you mean by standard cell approach ?

(*g*) Draw a CMOS-inverter.

(*h*) Explain the principle of CMOS latch-up.

2. Answer any *four* questions : 4 × 4

(*a*) Draw the flow diagram of typical VLSI design flow and explain. 2 + 2

(*b*) A microprocessor was fabricated in a 0·25 μm technology and was able to operate at 100 MHz, consuming 10 W using 2·5 V power supply. 2 + 2

(*i*) Using fixed voltage scaling, what will be the speed and power consumption of the same processor be if scaled to 0·1 μm technology ?

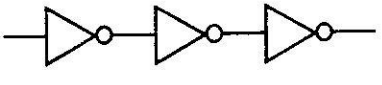
(*Continued*)

(*ii*) If the supply voltage on the 0·1 μm part were scaled to 1·0 V, what will be the power consumption and speed be ?

(*c*) Describe with a diagram the various charges associated with thermally grown oxidized silicon. 4

(*d*) What are the factors to be taken care for metallization in VLSI ? Estimate the intrinsic RC value of two parallel Al wires 0·5 μm × 0·5 μm in cross-section, 1 mm in length and separated by a polymide ($k = 2·7$) dielectric layer that is 0·5 μm thick. The resistivity of AL is 2·7 μΩ-cm. 2 + 2

(*e*) Draw the stick diagram of the following circuit : 2 + 2



(*f*) How design a SR flip flop using semi-custom methodology. 4

(*g*) Explain the CMOS inverter transfer characteristic highlighting the regions of operation of the MOS transistors. 4

(*h*) Describe the CMOS logic design. 4

3. Answer any *two* questions : 8 × 2

(*a*) (*i*) Draw the different capacitors involved in a MOS transistor.

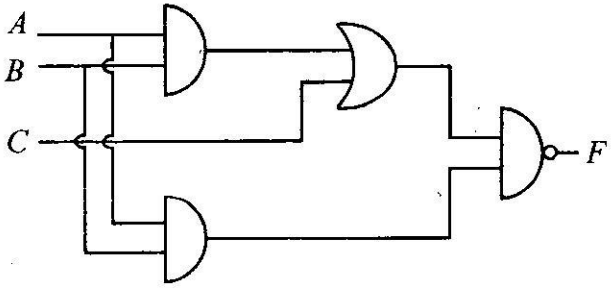
(*ii*) Draw and explain the MOS C-V characteristic for high and low frequency region. 3 + 5

(*b*) (*i*) What is the bird's beak structure in the oxidation process ? How is it prevented ?

(*ii*) If a silicon oxide of thickness x is grown in thermal oxidation, what is the thickness of silicon being consumed ? The molecular weight of silicon is 28·9 g mol^{-1}, and the density of Si is 2·33 g cm^{-3}. The corresponding values of SiO_2 are 60·08 g mol^{-1} and 2·21 g cm^{-3}. (2 + 2) + 4

(*c*) Describe with diagrams the steps followed in the fabrication of an *n*-channel enhancement mode MOSFET. 8

(*d*) Draw the CMOS circuit for the logic diagram shown below and find *F*. 8



[*Internal Assessment* : 10 Marks]