PG/IS/COS-102/19

M.Sc. 1st Semester Examination, 2019

COMPUTER SCIENCE

PAPER —COS-102

Full Marks : 50

Time : 2 hours

The figures in the right-hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

GROUP – A

1. Answer any *four* questions : 2 × 4

   (*a*) Compare von Neumann and Harvard architecture.

   (*b*) What is the difference between serial and parallel adder ?

(*c*) What is instruction format ?

(*d*) Distinguish hardware and microprogram control unit.

(*e*) What is I/O controller ?

(*f*) Compare and contrast linear and non-linear pipeline processor.

(*g*) Explain inclusion property of memory hierarchy.

(*h*) What is instruction pipeline ?

GROUP – B

2. Answer any *four* questions : 4 × 4

(*a*) Briefly explain SIMD architecture. 4

(*b*) Draw and explain COMA model of multiprocessor. What is the difference of it from UMA ? 3 + 1

(*c*) Explain with diagram the hardware control

unit. What is the advantage and disadvantage of such unit ? 2 + 2

(*d*) What is control hazard ? What is the solution to reduce such hazard of pipeline processor ? 2 + 2

(*e*) What is locality of reference ? Explain the different types of locality of reference. 4

(*f*) Draw and explain 4 bit adder subtractor. 4

(*g*) Compare between RISC and CISC. 4

(*h*) Explain any four types of addressing modes of instruction. 4

GROUP – C

3. Answer any *two* questions : 8 × 2

(*a*) (*i*) What is cache memory ?

(*ii*) Briefly explain hierarchical memory organization.

(*iii*) A hierarchical cache-main memory sub-

system has cache access time of 160 ns, main memory access time of 960 ns and hit ratio of cache memory of 0.9. Calculate average access time and efficiency of the memory system.

1 + 3 + 4

(*b*) Consider the following reservation table

Stages	Clocks 1	2	3	4	5	6	7
S_1	X		X				X
S_2				X		X	
S_3		X			X		

(*i*) Find all forbidden and non-forbidden latencies.

(*ii*) Draw state transition diagram.

(*iii*) List all simple and gredy cycles.

(*iv*) Calculate minimum average latency.

2 + 3 + 2 + 1

(Continued)

(*c*) (*i*) What is pipeline hazard ? Explain different types of data hazards.

(*ii*) Consider a 5 stage pipeline processor with clock rate of 10 MHz. Calculate speed up, efficiency and throughput for 5000 instructions. 4 + 4

(*d*) Explain any *two* of the following : 4 × 2

(*i*) Carry propagate adder

(*ii*) NUMA model of multiprocessor

(*iii*) Big and little endian

(*iv*) Virtual memory.

[*Internal Assessment* : 10 Marks]