2018

BCA 1st Semester Examination

DIGITAL ELECTRONICS LAB.

PAPER—1197 (Set-II)

(Practical)

Full Marks : 100

Time : 3 Hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer any *two* questions taking *one* from each group (lottery basis). 2×30

Group–A 1×30

1. Design a full adder using NAND gates only.

2. Implement basic gates using NOR gates only.

3. Implement Full-subtractor using 3×8 decoder and necessary gates.

4. Design 8×1 MUX using two 4×1 MUX and necessary gates.

5. Design a 2-bit comparator and verify its truth table.

6. Design an excess-3 to BCD code converter circuit and verify its truth table.

7. Design a 2-bit comparator and verify the truth table.

8. Design a 3 to 8 decoder and verify its truth table.

9. Design a circuit to convert BCD to excess-3.

10. Design a half subtractor using NAND gate and full subtractor using two half-subtractors.

Group–B

1×30

1. Design a D F/F using NAND gates and verify its output.

2. Design a Synchronous Counter 7 - 3 - 4 - 0 - 5 using J-K F/F and verify it.

3. Design a D F/F using J-K F/F and verify its truth table.

4. Design a Four bit (4-bit) Synchronous Counter.

5. Design a Synchronous Counter using J-K flip-flops to count the sequence 0-2-4-6-8-10-12-14.

6. Design a ripple counter using J-K flip-flop.

7. Design AND and OR operation using DTL and establish its truth table.

8. Design a asynchronous up counter of MOD 5.

9. Design and implement a right shift register and verify the output.

10. Design 4 bit SISO register using D flip-flop and verify the output.

Viva — 05

PNB — 05

Internal Assessment — 30