2018

BCA 1st Semester Examination

DIGITAL ELECTRONICS LAB.

PAPER—1197 (Set-I)

(Practical)

Full Marks : 100

Time : 3 Hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer any *two* questions taking *one* from each group (lottery basis). 2×30

Group–A 1×30

1. Design a half adder using NAND gates and verify its truth table.

2. Design a full subtractor using NOR gates and verify its truth table.

3. Design a 4 : 1 MUX using minimum number of NAND gates and verify its truth table.

4. Implement $Z = \overline{xy} + x + \overline{y + z}$ using NAND gates only and verify its truth table.

5. Design a half adder using NAND gates only and a full adder using two half adders.

6. Implement the following boolean function using a MUX :

$$F(A, B, C, D) = \sum (0, 1, 3, 4, 8, 9, 15).$$

7. Design a 1-bit comparator and verify its truth table.

8. Design a 4-bit 2's complement adder-subtractor using 7483 or an equivalent and X-OR gates.

9. Experimentally show that NAND gates and multiplexers are functionally complete.

10. Design a binary to gray code converter and verify its truth table.

Group–B

1×30

1. Design J-K master slave flip-flop and verify its execution table.

2. Design AND and OR operation using DTL and establish its truth table.

3. Design an asynchronous up counter (MOD 10).

4. Design a 4 bit SISO register using D flip-flop and verify its truth table.

5. Design and implement a right shift register and verify the operation.

6. Design an asynchronous up counter (MOD 5) using suitable gates.

7. Design a bi-directional 4-bit shift register using J-K F/F.

8. Design a 4-bit ripple counter using J-K F/F.

9. Design a synchronous counter to count 0 - 2 - 4 - 6 - 8 - 10 - 14 using J-K F/F.

10. Design a circuit to show the functional characteristics of a RAM chip (7489 or any other suitable chip).

Viva — 05

PNB — 05

Internal Assessment — 30

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