2018

BCA 1st Semester Examination

DIGITAL ELECTRONICS

PAPER—1104

Full Marks : 70

Time : 3 Hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the right-hand answers wherever necessary.

Answer Q. No. *1* and any *four* from the rest.

1. Answer any *five* questions : 5×2

(a) Convert the following decimal number to its octal equivalent $(0.640625)_{10}$.

(b) Simplify the following expression

$$Y = (A + B)(A + C')(B' + C').$$

(c) What is a Prime implicant ?

(d) Define Fan-in and Fan-out.

(e) What is Propagation delay ?

(f) State advantages and disadvantages of TTL.

(g) Define race around condition.

2. (a) Using k-map method to minimize the following expression :

$F(w, x, y, z) = m\,\Sigma(1, 5, 6, 12, 13, 14) + d\,\Sigma(2, 4)$. 8

(b) Implement EX-OR gate using NAND gate and NAND gate using NOR gate. 7

3. (a) Explain the concept of parity checking. 5

(b) Write down the 4-bit gray codes in the ascending order of decimal values starting from zero. 5

(c) Design a synchronous Mod-12 down counter using J-K flip-flop. 5

4. (a) Represent the decimal number "27" in

(i) BCD code

(ii) Octal code

(iii) Excess-3 code. 3

(b) Draw the block diagram of a digital multiplexer and explain its function. 4

(c) Give the functional truth table of a 4 : 1 multiplexer and realize it using gates AND, OR, NOT. 4

(d) Implement the expression using a multiplexer $f(A, B, C, D) = \Sigma m(0, 2, 3, 6, 8, 9, 12, 14)$. 4

5. (a) Design a BCD counter using JK flip-flop. 6

(b) Construct an SR (clocked) flip-flop using NAND gates. 4

(c) Design a Gray to Binery code converter. 5

6. (a) Describe Delta-encoded Digital to Analog converter. 5

(b) State the difference between SRAM and DRAM. 3

(c) State the difference between DTL and TTL. 2

(d) Explain Binary weighted Register DAC, R-2R non-inverting ladder DAC and R-2R inverting DAC in brief. 5

7. Write short note on any *three* of the following : 3×5

(a) Universal gates ;

(b) Decoder ;

(c) Shift Register ;

(d) Ripble counter ;

(e) Demultiplexer.
