NEW

2018

BCA

2nd Semester Examination

COMPUTER ORGANISATION AND ARCHITECTURE

PAPER—1201

Full Marks : 100

Time : 3 Hours

The figures in right-hand the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer Q. No. *1* and any *four* from the rest.

1. Answer any *five* questions. 5×2

(a) Draw a logic diagram of the Boolean function $f = \bar{A}B + C$.

(b) What is Universal gate ?

(c) What is the utility of accumulator ?

(d) What do you understand by micro program ?

(e) What is hit ratio ?

(f) Why data bus is bidirectional ?

(g) What is tri-state device ?

2. (a) What is instruction format ?

(b) Explain 'Immediate addressing' and 'relative addressing' technique.

(c) What is pipelining ? Explain the difference between RISC and CISC architecture. 3+(3+3)+(2+4)

3. (a) A block set-associative cache consists of a total of 64 blocks divided into four block sets. The main memory contains 4096 blocks, each consisting 128 words.

(i) How many units are there in a main memory address ?

(ii) What is the size of the cache memory ?

(b) Briefly explain the working principle of associative memory.

(c) Explain the difference between Micro-programmed and Hardwired control unit. 6+5+4

4. Explain the working of register set with common ALU with neat diagram. Explain the use of following register for a digital computer (any *three*) 6+(3×3)

   (i) MBR (ii) MAR (iii) PC (iv) IR.

5. (a) Explain with example of 'one address instruction' and 'O-address instruction'.

   (b) What do you mean by 'control memory' ?

   (c) What is DMA ? Explain the term

   (i) Bus request (ii) Bus grant (3+3)+3+(3+3)

6. (a) Draw the logic diagram of a 2 to 4 line decoder with NOR gates only.

   (b) Define the terms : seek time, Rotational delay and Access time in respect to memory.

   (c) What are the advantages of virtual memory ? 6+6+3

7. Write short notes (any *three*) : 3×5

   (a) RISC

(b) Memory Hierarchy

(c) Auxiliary Memory

(d) Sequential Circuit

(e) Common bus system.

[Internal Assessment—30 Marks]

———