2018

COMPUTER SCIENCE

[Honours]

PAPER – II

Full Marks : 90

Time : 4 hours

The figures in the right-hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

GROUP – A

Answer any two questions : 15 × 2

1. (*a*) Prove that following is a tautology

$$A \vee (\overline{B \wedge C}) \equiv (A \vee \overline{B}) \vee \overline{C}$$ 5

(*b*) Solve the recurrence relation

$$a_r - 3a_{r-1} + 2a_{r-2} = 0$$

satisfying the initial condition

$$a_0 = 1 \text{ and } a_1 = 4$$ 5

(*c*) Show that

$$\frac{1^2}{1.3} + \frac{2^2}{3.5} + \frac{n^2}{(2n-1)(2n+1)} = \frac{n(n+1)}{2(2n+1)}$$ 5

2. (*a*) Draw the circuit of two stage R-C coupled amplifier. Explain qualitatively nature of the frequency response characteristic of this amplifier. 8

(*b*) What is the effect on the space charge wilth at a *p-n*-Junction when the junction is (*i*) Forward biased and (*ii*) Reverse-biased. 7

3. (*a*) Describe the functions of each layers in OSI model. 7

(*b*) Explain the different types of ARQ techniques

in Data link layer with advantage and disadvantages. 8

4. (*a*) Explain how J-K flip-flop can be used for parallel data transfer. 5

(*b*) How does a MOSFET differ from a JFET ? Sketch the structure of an *n*-channel depletion-type MOSFET and briefly explain its working. Draw its circuit symbol. 1 + 4 + 1

(*c*) Design a logic circuit to implement binary to excess -3 code converter. 4

GROUP – B

Answer any five questions : 8 × 5

5. Using 4 bit parallel binary adder, design a circuit to perform BCD addition. Show different condition with different examples. 8

6. (*a*) What is meant by Common-Mode Rejection Ratio (CMRR) of an op-amp ? 2

(*b*) Explain the concept of virtual ground in

connection with op-amp. Draw the circuit diagram of a difference amplifier using op-amp and find an expression for the output voltage. 2 + 4

7. (*a*) Define conjunctive canonical form and disjunctive canonical form. 1 + 1

(*b*) What is the major restriction while operating a pulse triggered filp-flop ? 2

(*c*) An 8-to-1 Mux has inputs a, b, c connected to the selection inputs. The data inputs d_0 to d_7 are as follows $d_1 = d_2 = d_7 = 0$, $d_3 = d_5 = 1$, $d_0 = d_4 = d$ and $d_6 = d'$. Determine the Boolean expression that mux implements. 4

8. Explain HDLC frame format and how explain the concept of piggybacking used using HDLC frame during transmission. 8

9. Explain different types of switching techniques in brief. Compare and contrast between circuit switching and virtual circuits. 8

10. Write down the characteristics of zener diode. Describe the phenomenon of zener breakdown. 8

11. Reduce the expression using k-map and implement through minimum universal gates

$$f = \Pi M(2, 7, 9, 10, 11, 12, 14, 15) + d(0, 4, 6, 8)$$ 8

12. (*a*) Draw a block diagram of an 8 : 1 MUX. Design an 8 : 1 MUX using two 4 : 1 MUX and one 2 : 1 MUX. 4

(*b*) Draw the function

$F(D, C, B, A) = \Sigma m(0, 5, 7, 9, 10, 11, 13, 15)$

using 8 : 1 MUX. 4

GROUP – C

Answer any **five** questions : 4×5

13. What is bit stuffing and de-stuffing explain with example. 4

14. State and prove De Morgan's Law. 4

15. What is Router ? Differentiate function of Router, Switch and Hub. 4

16. Using set theory solve the following : 4

Among the first 500 positiver integers

(*a*) Determine the no of integers which are not divisible by 2, nor by 3, nor by 5.

(*b*) Determine the no of integers which are exactly divisible by one of them.

17. Define set and power set with example. 4

18. Write down the character of tri-state buffer. 4

19. A combinational circuit is defined by the following three functions :

$$f(x, y, z) = x'y' + xyz'$$

$$g(x, y, z) = x' + y \text{ and}$$

$$h(x, y, z) = xy + x'y'$$

Design the circuit with a decoder and external gates. 4

20. Fibonacci series can be described as 1, 1, 2, 3, 5, 8, ... α Formulate a recurrence relation defined on it. Hence solve that Recurrence relation for eliminating recursion using Generating Function. 4
