2017

BCA 1st Semester Examination

DIGITAL ELECTRONICS LAB.

PAPER—1197 (Set-I)

(Practical)

Full Marks : 100

Time : 3 Hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer any *two* questions taking *one* from each group (lottery basis). 2×30

Group–A 1×30

1. Design a half adder using NAND gates and verify its truth table.

2. Design a full subtractor using NOR gates and verify its truth table.

3. Design a two bit comparator circuit and verify its truth table.

4. Design a 4 : 1 MUX using NOR gates and verify its truth table.

5. Design 8 to 3 encoder circuit and verify its result using basic gates only.

6. Design a circuit to convert BCD to Excess-3.

7. Design a 4 : 1 MUX using minimum number of NAND gates and verify its truth table.

8. Design basic gates using minimum number of NAND gates.

9. Design a half adder using only NAND gates and a full adder using two half address.

10. Design a 8 : 1 Multiplexer and verify its truth table.

11. Implement $X = \overline{AB} + A + \overline{B + C}$ using only NAND gates and verify its truth table.

12. Design a 3 to 8 decoder and verify its result using 2 input basic gates.

13. Design AND, OR, NOT & X-OR gates using NAND gates.

14. Simplify the following function using K-map

$$F(A, B, C, D) = \Sigma_m(0, 1, 2, 5, 8, 9, 10)$$

and implement using basic gates.

15. Design binary to gray code converter and verify its truth table.

Group–B

1×30

1. Design 4 bit ripple counter using J-K F/F.

2. Design a 4 bit bidirectional Shift Register.

3. Design 4 bit SISO register using D F/F and verify the output.

4. Design asynchronous up counter of MOD 10 counter.

5. Design J-K master slave F/F and verify its execution table.

6. Construct clocked S-R flip-flop using NAND gates and verify its operation.

7. Design a J-K master slave flip-flop and verify its execution table.

8. Design S-R F/F using NAND gates.

9. Design a Buffer register and show the following result.

10. Design AND and OR operation using DTL and establish its truth table.

11. Design asynchronous upcounter (MOD 5) using suitable gates.

12. Design J-K F/F using NAND gates and verify its execution table.

13. Design a 4 bit ripple counter using J-K F/F.

14. Design AND and OR operation using DTL and establish its truth table.

15. Design and implement a right shift register and verify the operation.

Viva — 05 Marks

PNB — 05 Marks

Internal Assessment — 30 Marks