OLD

Part–III 3-Tier

2017

PHYSICS

(Honours)

PAPER—VII

(PRACTICAL)

Full Marks : 100

Time : 6 Hours

The figures in the right-hand margin indicate full marks.

Perform *one* expt. from Group—A and *one* expt. from Group-B.

Group—A (*Marks : 40*)

1. Design & construct a series regulated power supply using a pass transistor (power transistor) and a difference amplifier (a second transistor and a zener diode) to supply a maximum load current (< 500mA) at a specified voltage (voltage and current to be specified by the examiner). Take the data to draw the load regulation characteristics. Find the ripple factor at two different load currents and

no load condition at regulated region. (Here only capacitive filter can be used.)

To be supplied : h_{FE} of the power transistor,
h_{FE} of the 2nd transistor,
P_z (wattage) *and*
V_z (zener voltage of the zener diode).

Necessary calculations have to be done.

(a) Working formula. 3

(b) Ckt diagram. 4

(c) Calculations for the components. 6

(d) Implementation of the circuit. (*by the examiner*) 6

(e) Data for load regulation characteristics. (at least eight different currents) 8

(f) Drawing of load regulation characteristics. 5

(g) Data for ripple factor. 3

(h) Calculation of ripple factor. 3

(i) Discussions on load regulation characteristics and ripple characteristics. 2

2. Use the given OP-AMP as

(i) an inverting amplifier for gain 10 and

(ii) a non-inverting amplifier for gain 11.

In each case, study the variation of output voltage for different input voltages in the range −1V to +1V (*Null adjustment required*).

Take at least *ten* variations (reading) including +ve and -ve voltage in each case and plot the results.

Prepare the potential divider circuit to obtain the required input voltages.

(a) Working formula. 3

(b) Circuit diagram for inverting and non-inverting amplifier. $2\frac{1}{2}+2\frac{1}{2}$

(c) Circuit implementation. 4+4

(d) Preparation of potential divider circuit. 4

(e) Experimental data for V_{in} *vs.* V_o. 5+5

(f) Plotting the graphs. 3+3

(g) Calculate the experimental gain from graph for each cases. 2

(g) Discussion. 2

3. Design a CE-amplifier with a given transistor (*Given* : h_{FE}, h_{ie} and $(I_c)_{max}$ by the examiner) and study its linear characteristics (V_{in} *vs.* V_0) for a fixed frequency (*say*, 1 KHz) and study the frequency response (Gain *vs.* frequency) for a fixed input voltage (may be specified) and hence find the band-width of the amplifier.

Calculations for the components are to be done.

(a) Theory and Circuit. 3+3

(b) Calculation for the components. 5

(c) Implementation of the circuit. 5

(d) Data for linearity characteristics curve. 5

(e) Drawing of linearity characteristics curve. 4

(f) Data of the frequency response curve. 7

(g) Drawing of frequency response curve. 5

(h) Calculate the band-width for the amplifier. 2

(i) Calculate the mid frequency range of the amplifier. 1

4. Study the effect of negative feedback on frequency response of a RC-coupled amplifier (double stage : CE-CC) :

Implement a RC-coupled double-stage CE-CC amplifier on a bread-board using the specified (*given*) components and study the frequency response of the amplifier at the last-stage without and with negative feedback.

Input voltage may be specified by the examiner.

(a) Working theory. 4

(b) Circuit diagram. 4

(c) Implementation of the circuit. 6

(d) Verification of the biasing voltages at different nodes (Tabulate the voltage values). 4

(e) Data for frequency response without feedback. 6

(f) Data for frequency response with feedback. 6

(g) Drawing of frequency response curve for both with and without feedback (use semi-log graph paper). 4+4

(h) Calculate the bandwidth for the both cases. 2

5. Measure the (i) input off-set voltage, (ii) off-set current and (iii) input-bias currents of the given OP-AMP at gain 100 and 470.

Also perform the experiment for off-set null-adjustment.

(a) Theory and circuit diagram. 4+4

(b) Circuit implementation. 6

(c) Experimental results. 10

(d) Compare the results for two gain. 4

(e) Null-adjustment. 6

(f) Accuracy. 3

(g) Discussion in results. 3

6. Design and construct phase shift oscillator (amplitude limiter not required) for five different frequencies 500 Hz – 10 KHz (to be specified by the examiner). Compare the theoretical and experimental values of the frequency.

Measure the phase-shift due to RC network.

(a) Theory and Circuit. 4+3

(b) Calculation for the components. 5

(c) Implementation of the circuit. 7

(d) Experimental results. 10

(e) Table for theoretical and experimental values of the frequencies. 3

(f) Measurement of phase shift in each case at only one frequency. 6

(g) Discussion. 2

7. Design and construct Wien-bridge oscillator on a bread-board using OP-AMP for five different frequencies (to be specified by the examiners) in the range 500Hz – 10KHz. (amplitude limitation ckt. not required). Compare the theoretical and experimental values of the frequencies.

Measure the phase-shift for different frequencies at lead-lag network (by direct display on CRO screen).

(a) Theory and circuit diagram. 4+3

(b) Calculation for the components. 5

(c) Implementation of the circuit. 7

(d) Experimental results. 10

(e) Comparison with theoretical values of the frequency. 3

(f) Data for phase shift at lead-lag network. 5

(g) Discussion. 3

8. Adder and Subtracter :

Use the given OP-AMP as (i) an adder (3 input) and (ii) a subtracter (2 input) for gain 2 (for both cases).

Prepare the required sources for each cases.

Take at least five readings for each cases. Null adjustment should be done.

(a) Theory and circuit diagram. 4+4

(b) Preparation of source for input. 5

(c) Circuit implementation. 3+3

(d) Null adjustment. 3

(e) Experimental results. 5+5

(f) Comparison table for theoretical and experimental data. 3

(e) Accuracy. 2+2

(f) Discussion. 1

9. Integrator :

Use the given OP-AMP as an integrator (using sine-wave) and hence determine the value of the capacitance from frequency response curve.

(Unknown capacitance should be such that there would be f_0 ~ 160 Hz.)

(a) Theory and circuit diagram. 4+4

(b) Circuit Implementation. 5

(c) Measurement of the phase shift. (between input and output, for only three frequencies) 5

(d) Data for frequency response curve. 9

(e) Plotting of frequency response curve. 4

(f) Determination of capacitance. 4

(g) Accuracy. 3

(i) Discussion. [Null adjustment not required] 2

10. Differentiator :

Use the given OP-AMP as a differentiator and study the frequency response of the differentiator (using sine-wave) and hence determine the value of capacitance from the graph.

(Unknown capacitance should be such that the critical frequency would be $f_0 \sim 10$ KHz.)

Null adjustment not required.

(a) Theory and circuit diagram. 4+4

(b) Circuit implementation. 5

(c) Measurement of phase difference between input and output. (for at least three frequencies.) 5

(d) Data for frequency response. 9

(e) Plotting of frequency response. 4

(f) Determination of capacitance from graph. 4

(g) Accuracy. 3

(h) Discussion. 2

Group—B (*Marks : 40*)

(Attempt *one* expt.)

1. (a) Verify the following Boolean Expression using logic basic gates :

(output may be taken using voltmeter / multimeter / LEDs)

$$(A+B)(\bar{A}+C) = AC + \bar{A}B$$

(i) Draw the logic circuits. 6

(ii) Circuit implementation. 6

(iii) Truth table verification. 6

(iv) Discussion. 2

(b) Construct a half-adder circuit using only NAND gates and verify their truth tables :

(i) Theory and Circuit. 6

(ii) Circuit implementation. 6

(iii) Verification of truth table. 6

(iv) Discussion. 2

2. Construct a stable multivibrator (symmetrical) using transistor of frequencies 500Hz, 1KHz, 5KHz, 10KHz and 15KHz.

Draw the waveform at the collector and base of any one transistor. Compare the calculated and the experimental values of the frequencies :

(a)	Theory and circuit diagram.	3+3
(b)	Calculation for the components.	5
(c)	Circuit implementation.	5
(d)	Experimental results.	10
(e)	Drawing of the waveforms. (for one frequency.)	4+4
(f)	Comparison of experimental and theoretical values of the frequencies.	2
(g)	Accuracy.	3
(h)	Discussion.	1

3. Construct an astable multivibrator using IC-555 to generate symmetrical square-wave of frequencies 500Hz, 1KHz, 5KHz, 10KHz and 15KHz.

Compare the experimental values of frequency with theoretical values. Draw the output waveform at any two of the above frequencies.

(a)	Theory and circuit diagram.	3+3
(b)	Calculation for the components.	5
(c)	Circuit implementation.	5
(d)	Experimental results.	10
(e)	Comparison of frequencies with theoretical values.	3
(f)	Drawing of output waveform. (for two frequencies)	6
(g)	Accuracy.	3
(h)	Discussion.	2

4. (a) Use NAND gates to construct OR and AND gate :

(i) Draw logic circuits. 3+2

(ii) Implementation of the circuits. 3+2

(iii) Verification of truth table. 4+3

(output may be taken using voltmeter / multimeter / LEDs.)

(b) Design a 1:4 demultiplexer using basic gates and represent its performance in a table and conclude the results :

(i) Theory. 3

(ii) Logic circuit diagram. 3

(iii) Circuit implementation. 9

(iv) Data recording. 5

(v) Conclusion. 3

5. (a) Construct AND and OR gates using diodes and resistors and NOT gate using transistor (h_{FE} of the transistor will be supplied) and verify their truth tables :

(i) Truth tables and circuit diagram. 6

(ii) Circuit for NOT gate. 3

(iii) Circuit implementation. 2×3

(iv) Experimental Results and Verification of Truth tables. 3×3

(b) Use NAND gates (IC-7400) to construct two-input OR, AND and NOT gate :

(i) Circuit diagram. 3

(ii) Circuit implementation. 2+3+2

(iii) Results and the corresponding truth tables. 6

6. (a) Design a 4:1 multiplexor using basic gates and represent its performance in a table and write the conclusion about its performance :

(i) Theory. 4

(ii) Logic circuit diagram. 4

(iii) Circuit implementation. 7

(iv) Data recording. 5

(v) Conclusion and remarks. 3

(b) Verify the following Boolean Expression using basic IC gates :

$(A + B)(B + C)(C + A) = AB + BC + CA$

(output may be taken using voltmeter / multimeter / LEDs)

(i) Draw logic circuits. 6

(ii) Implementation of the circuits. 6

(iii) Verification of the truth table. 5

7. (a) Construct a full-adder circuit using basic gates and verify truth tables :

(i) Theory and Circuit. 4+4

(ii) Circuit implementation. 8

(iii) Verification of truth table. 8

(b) Use NAND gates to construct OR and AND gate :

(i) Draw logic circuits. 3+2

(ii) Implementation of the circuits. 3+2

(iii) Verification of truth table. 3+3

8. (a) A block of 20 bytes of data are stored at data-memory location starting from X. Copy a block of data without disturbing the order to data location starting from Y.

(b) Subtract from any hexadecimal no. to a 2nd number (given by the examiner) so that the first number (given by the examiner) is in the memory location y and the 2nd number is in the memory location y + 1, whole the result of subtraction is to be stored in the memory location y+2.

(memory location will be assigned by the examiners.)

(i) Programming. 6×2

(ii) Storing, execution of the program and results (result table should be drawn). 14×2

9. (a) Four bytes of data are specified at consecutive data memory locations starting at location X. Write a program which increments the values of all data bytes by two (in the same memory locations).

(i) Programming. 6

(ii) Storing, execution of the programme and results (result-tables are to be shown with proper comments.) 14

(b) Store two hexadecimal number (given by the examiner) at memory locations X and (X+1) (may be specified by the examiner) of 8085 microprocessor. Write a program to compute the sum of the above two numbers and store the result at location (X+2) (specified by the examiner); ignoring the possible overflow.

(value of X will be specified by the examiner.)

(i) Programming. 6

(ii) Storing, execution of the programme and results (result-table are shown with proper comments.) 14

10. Design the following flip-flops using NAND-gates only and verify their truth-table :

(a) Clocked-SR-flip-flop ;

(b) JK-flip-flop.

(i) Theory. 3+3

(ii) Circuit diagram. 3+4

(iii) Circuit implementation. 4+6
(For JK flip-flop, truth-table must be verified for all possible combination of inputs and as well as outputs.)

(iv) Truth table verification. 5+12

11. Design asynchronous up-counter of following mods using IC-7476 (JK–MS–FF) :

(i) Mod 7, (ii) Mod 5 and (iii) Mod 3
and represent their operation in table.

(i) Theory and circuit. 4+4

(ii) Circuit implementation. 8

(iii) Experimental data. 7×3

(iv) Discussion. 3

INSTRUCTIONS

Distribution of marks :

Laboratory Note Book		:	10
Viva		:	10
Experiments	Gr. A	:	40
	Gr. B	:	40
	Total	:	100

1. Two experiments, taking one from Group–A and another from Group–B, are to be performed by each candidate.
2. Selection of experiment has to be done through lottery or drawing cards (separately for Group–A and Group–B).
3. In generally, two chances are to be given to each candidate to draw card, or to take part in the lottery by rotation.
4. Third and the last chance may be allowed by deducting 3 marks (for each group).
5. The circuit diagram and working formula, may be supplied to the candidate, who are unable to write or draw the same. In that case, marks for the corresponding items are to be deducted by the examiner on duty.
6. Examiners should be aware of the instrumental disturbances but in ni case, any kind of help in implementing the circuit is allowed. The candidate has to implement the circuit by their own, strictly.
7. Marks on the LNB will be given proportionately to the number of experiments performed properly and be presented with proper sign by the teachers of the college concerned. Full-marks (i.e. 10) will be given to the candidate who performed at least ten experiments in Group–A and ten experiments in Group–B.

   (OP–AMP experiments, Digital experiments and multivibrator experiments can be considered as separate experiments.)
8. Time for Group–A = 3 hrs.

   Group–B = 3 hrs.

   (*not strictly*)
9. Try to set each experiment.
10. In case of any ambiguity relating to questions or evaluation, concerned Head Examiner may be contacted.

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