UG/I/CSC/H/II/17

2017

COMPUTER SCIENCE

[Honours]

PAPER –II

Full Marks : 100

Time : 4 hours

The figures in the right hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

GROUP – A

Answer any two questions : 15 × 2

1. (*a*) Find the truth table for

$$(P \rightleftarrows \neg Q) \rightleftarrows (Q \rightarrow P)$$ 5

(*b*) Solve

$$a_n = 4a_{n-1} - 4a_{n-2} + n2^n$$

where $a_0 = 1$ and $a_1 = 3$. 5

(*c*) Show that

$$\sum_{i=0}^{n-2} 2^{n-2-i}(n-1-i) = (n-2)2^{n-1} + 1$$

using mathematical induction. 5

2. (*a*) What is IP address ? Discuss about the structure of class C IP address format. 5

(*b*) With a neat diagram draw and explain the basic structure of an *n*-channel JFET. 5

(*c*) Let

$A = \{1, 2, 3, 4\}$ and $R = \{(1, 1), (1, 2), (1, 3), (2, 1), (2, 2), (2, 3), (3, 1), (3, 2), (3, 3), (4, 4)\}$.

Is R an equivalence relation ? If yes Find the partition of A induced by R. 5

3. (*a*) Draw and describe the two bit comparator circuit. 6

(*b*) Prove that

$$AB + B(B + \bar{C}) + \bar{B}C = B + C$$ 4

(*c*) Design and explain the 4-bit adder-cum substractor circuit. 5

4. (*a*) Define Latch. Describe NOR based S-R Latch. 1 + 4

(*b*) What do you mean by asynchronous counter ? 5

(*c*) Write down the functions of the physical layer and network layer in ISO/OSI reference model. $2\frac{1}{2} \times 2$

GROUP – B

Answer any **five** questions : 8×5

5. Explain the operation of a bidirectional shift register. 8

6. Use Boolean algebra to simplify the following Boolean expression and implement in NAND logic

$$f(A,B,C,D) = \sum m(10,11,14,15)$$ 8

7. Let $f: R \to R$ be defined by $f(x) : 3x + 1, x \in R$. Examine it f is (*i*) Injective (*ii*) Surjective. 8

8. Write down the difference characteristic of zener diode. Describe the phenomenon of zener break down. 8

9. (*a*) A channel has a bit rate of 4 kbps and a propagation delay of 20 msec. For what range of frame size does stop and wait protocol give an efficiency of at least 50%. 3

   (*b*) Explain the basic feature of link state routing. 5

10. Discuss about the principle of operation of a crystal-Oscillator ? Write down the two advantages of it ? 6 + 2

11. (*a*) How parity bits are used to detect the error in transmission of data ? 6

(*b*) What is DNS ? 2

12. Explain different modes of data flow in data communication. What is protocol. 6 + 2

GROUP – C

Answer any **five** questions : 4 × 5

13. State and prove De-Morgan's theorem. 4

14. Explain briefly any one kind of guided media used in transmission medium ? 4

15. Write down the characteristics of tri-state buffer. 4

16. What is multiplexing ? Describe FDM and WDM. 4

17. What is bistable multivibrator ? Draw it's block diagram. 4

18. Define set and power set with proper example. 4

19. What is congestion ? How does it occurs ? 4

20. Draw HDLC frame structure. 4

[*Internal Assessment* : 10 Marks]
