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Realization of Third-Order Voltage-Mode/Current-Mode Quadrature Oscillator Circuit Employing VDCCs and All Grounded Capacitors

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ABSTRACT

A new configuration of voltage-mode/current-mode (VM/CM) third-order quadrature oscillator is proposed in this article. The proposed third-order oscillator employs two voltage differencing current conveyors (VDCCs), three grounded capacitors and three resistors of which two are grounded. The use of grounded capacitors makes the circuit suitable for IC implementation. This particular circuit provides two voltage-mode and two current-mode sinusoid signals with 90^o phase difference. The frequency of oscillation (FO) and condition of oscillation (CO) are independently controllable through single grounded passive element. The FO and CO can also be tuned electronically. The workability of the oscillator circuit is tested through PSPICE simulation using 0.18 µm TSMC CMOS process parameters. The total harmonic distortion is found to be nearly 1%. The static power dissipation is 1.35 mW for ± 0.9 V power supply. Non-ideal as well as parasitic analysis of the designed circuit has been carried out to strengthen the design idea. Monte-Carlo analysis result has also been included.

Keywords: Third-Order Quadrature Oscillator, Current-Mode (CM), Voltage-Mode (VM), Voltage Differencing Current Conveyor (VDCC).

1. Introduction

Quadrature oscillator is an important block as it provides two sinusoids with 90^o phase difference and widely used in signal processing, telecommunication, control systems, measurement systems and instrumentation [1, 4, 6]. It is well known that the higher-order network provides high quality factor, high accuracy and better frequency response with minimum distortions. So, third-order quadrature oscillator (TOQO) which has third-order polynomial regression is a better choice than the second order quadrature oscillator (SOQO).

Recently, a number of TOQO based on various active building blocks (ABBs) has been reported [5, 7, 9–11, 16–21, 24]. These oscillator circuits, however, have some limitations and problems. Maheshwari in [19] reported a third-order quadrature oscillator circuit. But the circuit uses three current controlled current conveyor (CCCII) blocks. Using two second generation current conveyors (CCIIs), three capacitors and three resistors, Horng in [10] proposed a VM/CM third-order oscillator but a comparatively

large supply voltage is required to drive this circuit. Two quadrature sinusoidal oscillators employing CMOS operational transconductance amplifier (OTA) was proposed by Pipat Prommee and Kobchai Dekhan in [24]. But their circuits require three and four OTAs for first and second circuit respectively and also provide only voltage outputs. Montree Kumngern and Ittipol Kansiri in [17] proposed a third-order quadrature oscillator using operational transresistance amplifier (OTRA). But they use three OTRAs and all floating capacitors and resistors. Nagar et al. also proposed two third-order quadrature oscillator circuits employing two OTRAs in [20], but both the circuits utilize three floating resistors and three floating capacitors. The circuits also provide only voltage-mode outputs. Based on third-order technique Duangmalai et al. reported a quadrature oscillator in [7], but the circuit is designed using two different blocks—current controlled current conveyor transconductance amplifier (CCCCTA) and operational transconductance amplifier (OTA). The circuit also provides only current-mode outputs. Again, Montree Kumngern and Somyot Junnapiya reported a third-order quadrature oscillator in [16], but the circuit is also designed by using mixed blocks—current-controlled current differencing transconductance amplifier (CCCDTA) and operational transconductance amplifier (OTA). In addition, this circuit does not provide voltage output. A third-order oscillator structure with current/voltage output was proposed by Bhartendu Chaturvedi and Sudhanshu Maheshwari using differential voltage current conveyor (DVCC) [5], but the circuit requires three active building blocks (ABBs). In [11], Horng et al. proposed a VM/CM third-order oscillator circuit using current differencing transconductance amplifiers (CDTAs) and three grounded capacitors. But three CDTAs are needed for this circuit. Again, Jiun-Wei Horng reported a third-order quadrature oscillator based on CDTA [9]. But the circuit employs three CDTAs and provides only current outputs. Kritphon Phanruttanachai and Winai Jaikla reported a third-order quadrature oscillator in [21], but the circuit uses two different active blocks, namely—voltage differencing transconductance amplifier (VDTA) and differential difference current conveyor (DDCC). Also, this circuit suffers the limitation of operating only on current-mode. The third-order quadrature oscillator reported in [18] also uses mixed building blocks—one DDCC and two OTAs. The circuit has also the limitation of operating only on voltage-mode. A qualitative comparison between the proposed and previously reported oscillator circuits is shown in Table 1.

Lately, the voltage differencing current conveyor (VDCC) has appeared as an attractive analog building block reported by Biolek in 2008 [3]. It offers electronically tunable transconductance gain along with the capability of transferring both the current and voltage to the relevant terminals. Several analog circuits, such as, inductive simulator [15, 22, 28], filter [12–14], second order oscillator [8, 23, 27, 29] etc., using VDCC as active element are reported in literature, but there is no TOQO based on VDCC. This encourages the authors to report a new TOQO employing VDCC as an active element.

The aim of this paper is to offer a third-order quadrature sinusoidal oscillator circuit based on VDCCs and all grounded capacitors, which provides following advantageous features, such as:

- Suitable for monolithic implementation; as all the capacitors used in the circuit are grounded.
- Both the voltage-mode and the current-mode quadrature outputs are available in the circuit.

- ❖ The frequency of oscillation (FO) and condition of oscillation (CO) can be tuned independently by the use of single grounded passive element. In spite of that, we can also tune electronically the FO and CO under proper condition.
- ❖ All the active and passive sensitivities of the circuit are found to be low.

Ref.	**No. of Active element**	**No. of R+C Grounded (G) /Floating(F)**	**VM/CM output**	**Technology**	**Supply voltage (V)**	**Uncoupled FO and CO**	**THD (%)**
[5]	3 DVCC	3(2G,1F) +3(G)	both	0.5 µm	± 2.5 V	yes	≤2
[7]	1 CCCCTA, 1 OTA	0+3(G)	current	NA	± 2 V	yes	1.09
[9]	3 CDTA	0+3(G)	current	0.18 µm	± 1.25	yes	2.57
[10]	2 CCII	3(2G, 1F)+3(G)	both	0.18 µm	± 1.25 V	yes	2.95
[11]	3 CDTA	0+3(G)	both	0.18 µm	± 1.25	yes	10.39
[16]	1 CCCDTA 1 OTA	0+3(G)	both	0.25 µm	± 1.5 V	yes	1.8
[17]	3 OTRA	5(F)+3(F)	voltage	0.25 µm	± 2.5 V	yes	4.82
[18]	1 DDCC 1 OTA	1(G)+3(G)	voltage	0.25 µm	± 1.25	yes	1.75
[19]	3 CCCII	0+3(G)	both	0.5 µm	± 2.5 V	yes	1.927
[20]	Fig.2d. 2 OTRA Fig. 3d. 2 OTRA	3(F)+3(F)	voltage	0.5 µm	± 1.5 V	yes	1.17 1.32
[21]	1 DDCC 1VDTA	1(G) +3(G)	current	0.25 µm	± 1.25	yes	2.95
[24]	Fig.7.b. 3 OTA Fig.11. 4 OTA	0+3(G) 1(G)+3(G)	voltage	ES-2-MODEL	± 3 V	yes	not given
This work	2 VDCC	3(2G,1F)+3(G)	both	0.18 µm	± 0.9	yes	≤1

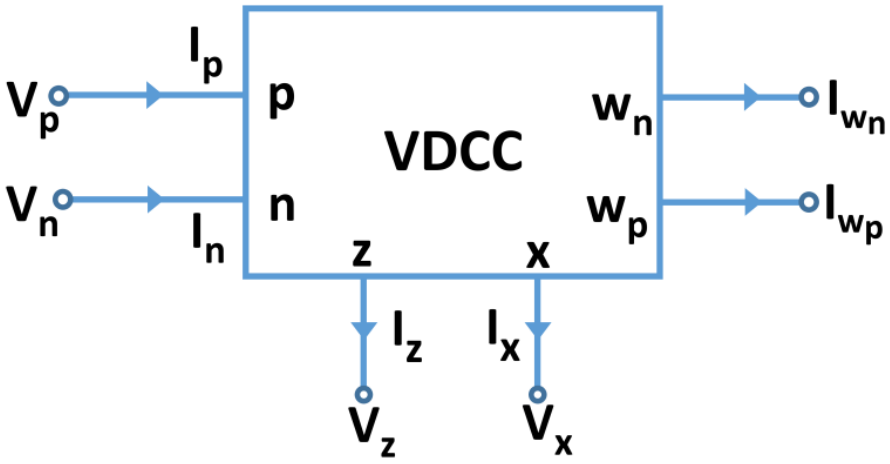
Table 1: Comparison between the proposed oscillator and previously informed works

The rest portion of the paper is divided as follows: The proposed circuit has been described in Section 2. Performance of the circuit under non-ideal condition has been given in Section 3. This section also gives the sensitivity analysis of the circuit. In Section 4, the effects of the parasitics of the VDCC on the proposed circuit have been discussed. Sections 5 present the PSPICE simulation results. The conclusion of the paper has been presented in Section 6.

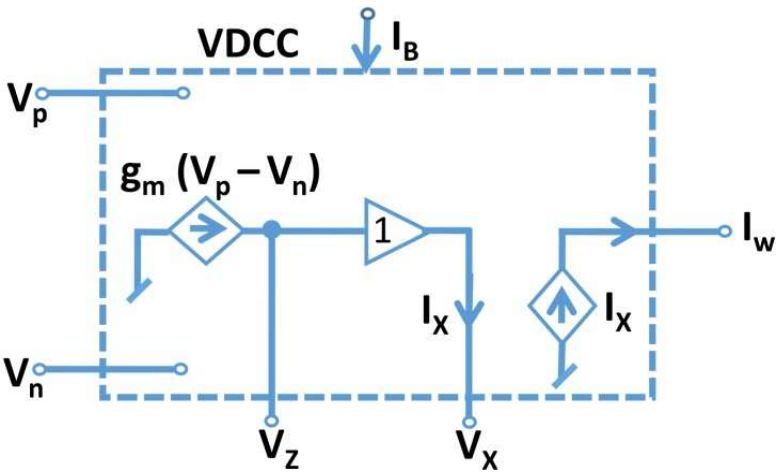
2. Circuit description

2.1. Voltage differencing current conveyor (VDCC)

VDCC is a versatile active building block which is basically a combination of OTA and CCII. It inherits all the properties of current-mode active element, such as, higher speed, low power consumption, higher slew rate, better linearity etc. [25, 26]. Fig. 1a represents the block diagram of the VDCC, where p and n are input ports and z, x, w_p and w_n are output ports. The ports z, w_p and w_n offer high impedances whereas x is the low impedance port. The equivalent circuit of this particular active block has been demonstrated in Fig. 1b.



(a)



(b)

Figure 1: The VDCC (a) block diagram (b) equivalent circuit

The ideal characteristic equation of VDCC is given by equation (1):

$$I_p = 0, I_n = 0, I_z = g_m(V_p - V_n), V_x = V_z \text{ and } I_{wp} = -I_{wn} = I_x \quad (1)$$

where g_m is the transconductance gain of VDCC. For CMOS VDCC, g_m is electronically tunable by DC bias current and defined by

$$g_m = \sqrt{I_B \mu_n C_{ox} \left(\frac{W}{L}\right)} \tag{2}$$

where I_B is the bias current, μ_n is the mobility of the carrier for the NMOS transistors, C_{ox} is the gate-oxide capacitance per unit area, and $\frac{W}{L}$ is the aspect ratio of MOSFET [23]. The CMOS structure of VDCC has been demonstrated in Fig. 2 [29].

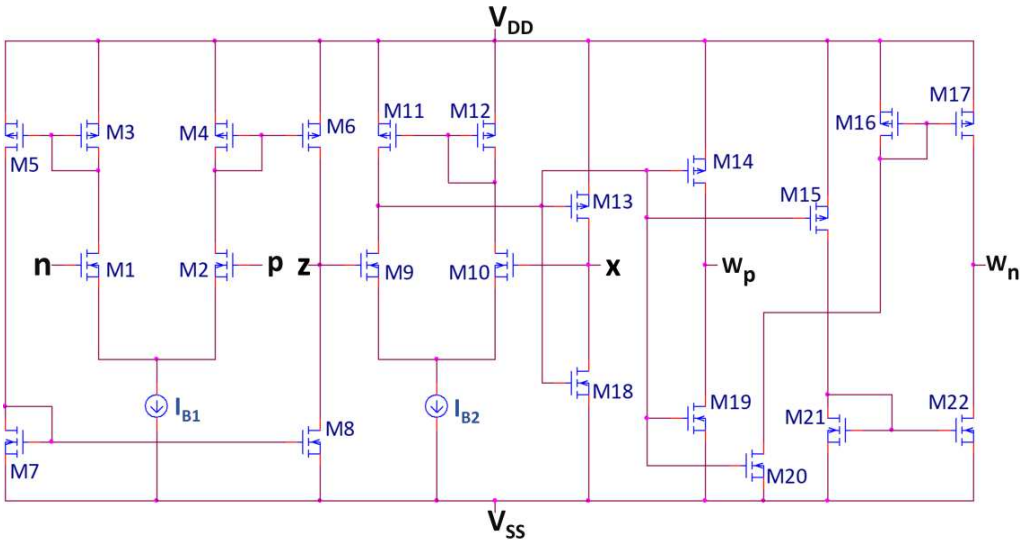


Figure 2: Internal structure of CMOS VDCC [29]

2.2. Proposed quadrature oscillator circuit

Fig. 3 represents the schematic diagram of the proposed third-order quadrature oscillator circuit. As shown in Fig. 3 it employs two VDCCs, three grounded capacitors, and three resistors of which two are grounded.

The characteristic equation of the proposed oscillator circuit can be expressed as:

$$s^3 R_1 R_3 C_1 C_2 C_3 + s^2 g_{m1} R_2 R_3 C_2 C_3 + s g_{m1} R_3 C_3 + g_{m1} g_{m2} R_1 = 0 \tag{3}$$

From equation (3), frequency of oscillation (FO) and condition of oscillation (CO) can be expressed as:

$$\text{FO: } f_0 = \frac{1}{2\Pi}\sqrt{\frac{g_{m1}}{R_1 C_1 C_2}} \tag{4}$$

$$\text{CO: } g_{m2} \leq \frac{g_{m1} R_2 R_3 C_3}{{R_1}^2 C_1} \tag{5}$$

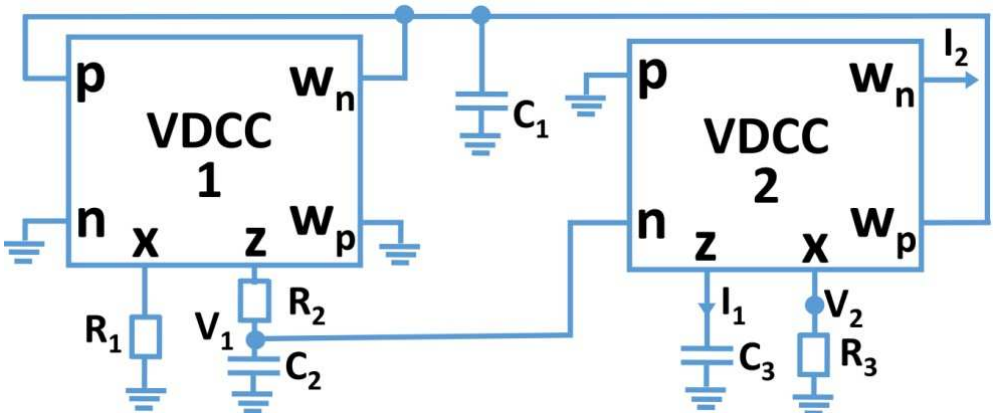


Figure 3: Proposed VM/CM quadrature oscillator circuit

From the circuit of Fig. 3, the voltage ratio of V_2 & V_1 and the current ratio of I_2 & I_1 are found to be as follows:

$$\frac{V_2(s)}{V_1(s)} = -\frac{g_{m2}}{sC_3} \tag{6}$$

$$\frac{I_{2(s)}}{I_1(s)} = -\frac{1}{sC_3R_3} \tag{7}$$

Under sinusoidal steady state, equations (6) and (7) become

$$\frac{V_2(j\omega)}{V_1(j\omega)} = \frac{g_{m2}}{\omega C_3} e^{j90^o} \tag{8}$$

$$\frac{I_2(j\omega}{I_1(j\omega)} = \frac{1}{\omega C_3R_3} e^{j90^o} \tag{9}$$

From equations (8) and (9) it is clear that the phase difference between V_2 and V_1 and I_2 & I_1 is 90^o. This indicates that the circuit can works as a VM/CM quadrature oscillator. From equations (4) and (5) it is also clear that the FO and CO of the reported circuit can be tuned independently without affecting each other (FO by using C_2 and CO by using C_3 *or* R_2 *or* R_3). In addition to this, it is also clear from equations (4) and (5) that we can also tune this circuit electronically if we first tune the value of FO by using g_{m1} and then adjust the CO by using g_{m2}.

3. Non-ideal and sensitivity analysis

Considering the non-ideality errors of the VDCC, equation (1) can be rewritten as:

$$\left.\begin{aligned} I_p = 0,\ I_n = 0,\ I_z = \alpha_i g_{mi}(V_p - V_n), V_x = \beta_i V_z,\ I_{wp} = \gamma_{pi} I_x \\ \text{and}\ \ I_{wn} = -\gamma_{ni} I_x \end{aligned}\right\} \tag{10}$$

where $\alpha_i, \gamma_{pi}, \gamma_{ni}$ represent the current tracking errors and β_i represents the voltage tracking error of the *i*-th VDCC.

Reanalysing the circuit of Fig. 3 on the basis of equation (10), the characteristic equation becomes:

$$s^3C_1C_2C_3R_1R_3 + s^2\alpha_1\beta_1\gamma_{n1}C_2C_3R_2R_3g_{m1} + s\alpha_1\beta_1\gamma_{n1}g_{m1}R_3C_3 + \alpha_1\alpha_2\beta_2\gamma_{p2}g_{m1}g_{m2}R_1 = 0 \tag{11}$$

From equation (11), the FO and CO of the proposed circuit can be found as:

$$\text{FO: } f_0 = \frac{1}{2\Pi}\sqrt{\frac{\alpha_1\beta_1\gamma_{n1}g_{m1}}{R_1C_1C_2}} \tag{12}$$

$$\text{CO: } g_{m2} \leq \frac{\alpha_1\beta_1^2\gamma_{n1}^2R_2R_3C_3g_{m1}}{\alpha_2\beta_2\gamma_{p2}R_1^2C_1} \tag{13}$$

It is evident from equations (12) and (13) that the FO and CO of the devised oscillator are slightly deviated under non-ideal condition. However, the FO and CO are still separately controllable (FO by C_2 and CO by C_3 or R_2 or R_3 or α_2 or β_2 or γ_{p2}).

Under non-ideal conditions, the sensitivities with respect to various active and passive elements are expressed in equation (14):

$$s^{f_0}_{\alpha_1,\beta_1,\gamma_{n1},g_{m1}} = -\,s^{f_0}_{R_1,C_1,C_2} = \frac{1}{2} \text{ and } s^{f_0}_{\alpha_2,\beta_2,\gamma_{p1},\gamma_{p2},\gamma_{n2},R_2,R_3,C_3,g_{m2}} = 0 \tag{14}$$

So, equation (14), confirms that under non-ideal conditions all the sensitivities of the devised oscillator circuit are not more than $\frac{1}{2}$ in magnitude. Thus, the sensitivity of the proposed third-order quadrature oscillator is under considerable limits.

From the above discussion it may concluded that the designed circuit can behave excellently even under non-ideal conditions.

4. Effects of VDCC parasitics

Fig. 4 displays the parasitic model of VDCC [8]. Including the parasitics of VDCCs, the proposed circuit has been replicated in Fig. 5.

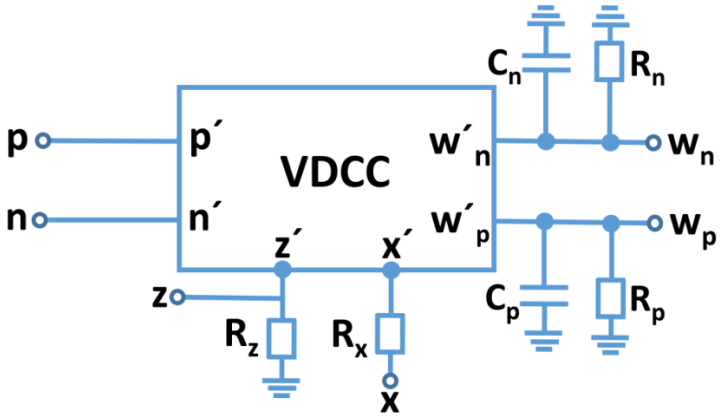


Figure 4: Parasitic model of VDCC [8]

In Fig. 5; $R_a = R_1 + R_{x1}, R_b = R_{n1} || R_{p2}$ and $C_a = C_1 + C_{p2} + C_{n1}$.

The characteristics equation of the circuit of Fig. 5 can be expressed as:

$$\alpha s^3 + \beta s^2 + \gamma s + \delta = 0 \tag{15}$$

where $\alpha = R_aC_2C_3C_a$, $\beta = \left\{ R_aC_3\left(\frac{C_a}{R_c} + \frac{C_2}{R_b}\right) + C_2\left(\frac{R_aC_a}{R_{z2}} + \frac{g_{m1}R_2R_{z1}C_3}{R_c}\right)\right\}$,

$$\gamma = \left\{\frac{g_{m1}R_{z1}}{R_c}\left(C_3 + \frac{R_2}{R_{z2}}C_2\right) + \frac{R_a}{R_c}\left(\frac{C_3}{R_b} + \frac{C_a}{R_{z2}}\right) + \frac{R_aC_2}{R_bR_{z2}}\right\},$$

and $\delta = \left\{\frac{g_{m1}R_{z1}}{R_c}\left(\frac{g_{m2}R_a}{R_d}+\frac{1}{R_{z2}}\right)+\frac{R_a}{R_bR_cR_{z2}}\right\}$.

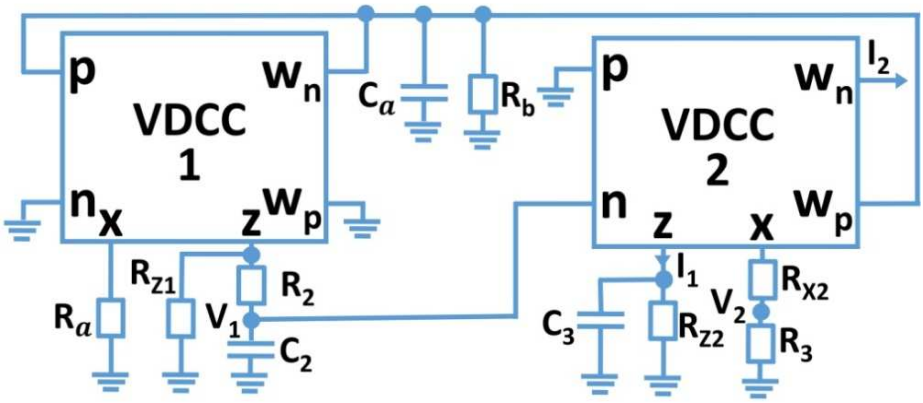


Figure 5: The proposed oscillator circuit with the parasitic of VDCCs

Thus the expression of FO and CO of the proposed circuit can be modified as:

$$\text{FO: } f_0 = \frac{1}{2\Pi}\sqrt{\frac{g_{m1}}{\left(1+\frac{R_2}{R_{z1}}\right)R_aC_aC_2}+\frac{g_{m1}R_2}{\left(1+\frac{R_2}{R_{z1}}\right)R_aR_{z2}C_aC_3}+\frac{1}{R_cR_{z2}C_2C_3}+\frac{1}{R_bR_{z2}C_aC_3}+\frac{1}{R_bR_cC_aC_2}} \quad (16)$$

$$\text{CO:}\frac{g_{m1}^2R_2}{\left(1+\frac{R_2}{R_{z1}}\right)^2R_aC_a}\left(C_3+\frac{R_2C_2}{R_{z2}}\right)+\frac{g_{m1}}{\left(1+\frac{R_2}{R_{z1}}\right)}\text{X}+\frac{g_{m1}}{\left(1+\frac{R_2}{R_{z1}}\right)}Y+\text{Z} \geq \frac{g_{m1}g_{m2}R_a}{\left(1+\frac{R_2}{R_{z1}}\right)R_d} \quad (17)$$

where $\text{X} = \left(\frac{C_3}{R_bC_a}+\frac{2R_2C_2}{R_{z2}R_bC_a}+\frac{R_2C_2}{R_{z2}^2C_3}\right)$, $\text{Y} = \frac{1}{R_c}\left(\frac{2R_2}{R_{z2}}+\frac{C_3}{C_2}+\frac{R_2C_3}{R_bC_a}\right)$,

$$\text{Z} = \frac{R_a}{R_c}\left[\frac{1}{R_b}\left(\frac{C_3}{R_bC_a}+\frac{2}{R_{z2}}\right)+\frac{C_a}{R_{z2}^2C_3}\right]+\frac{R_a}{R_c^2C_2}\left(\frac{C_3}{R_b}+\frac{C_a}{R_{z2}}\right)+\frac{R_aC_2}{R_bR_{z2}}\left(\frac{1}{R_bC_a}+\frac{1}{R_{z2}C_3}\right),$$

$$R_c = R_2 + R_{z1}, \text{ and } R_d = R_3 + R_{x2}\,.$$

It is evident from equations (16) and (17) that the FO and CO of the devised oscillator are affected by the parasitics of the VDCCs. However, this is not adverse as the value of the parasitic resistances $R_{z1,}\,R_{z2}$ and R_c are very high [14].

5. Simulation results

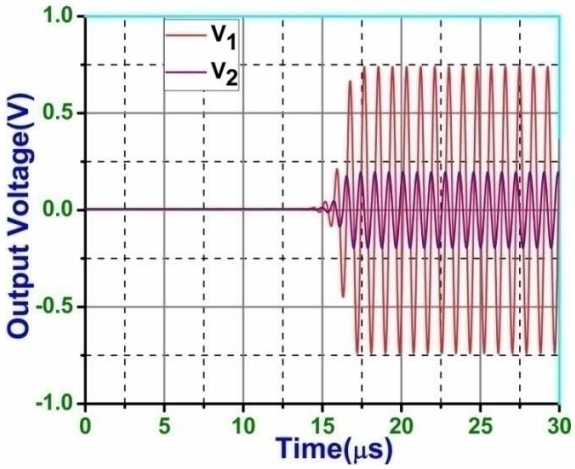
The reported third-order quadrature oscillator has been simulated with Cadence OrCAD PSPICE simulator using the parameters of a 0.18 µm CMOS technology of Taiwan Semiconductor Manufacturing Company, Ltd. [2] to test the theoretical analysis. The supply voltages are taken as $V_{DD} = -V_{SS}$ = 0.9 V and the biasing currents are taken as I_{B1} = 50 μA and I_{B2} = 100 μA (g_m = 277.8 μA/V). The aspect ratios of the MOS transistors used in Fig. 2 is presented in Table 2 [29].

The circuit was simulated using R_1 = R_2 = R_3 = 1 kΩ, C_1 = C_3 = 68 pF, and C_2 = 75 pF. The value of theoretical frequency of this design was 1.17 MHz, whereas the value of simulated frequency was found as 1.12 MHz. The deviation is just 4.27%. The initial and steady state waveforms for the quadrature voltage outputs V_1 and V_2 are shown in Fig. 6a and Fig. 6b respectively. The same for the quadrature current outputs I_1 and I_2

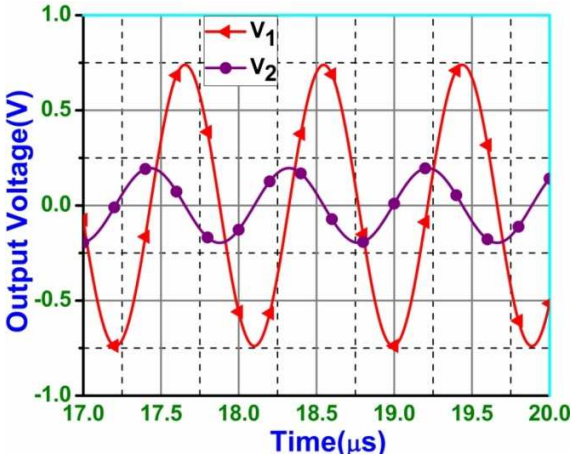
are shown in Fig. 7a and Fig. 7b respectively. It is clear from the Fig. 6a and Fig. 7a that the circuit takes 17.65 µs to start its steady operation.

Transistor	W/L (µm)
M1, M2, M3, M4	3.6/1.8
M5, M6	7.2/1.8
M7, M8	2.4/1.8
M9, M10	3.06/1.72
M11, M12	9.0/1.72
M13, M14, M15, M16	14.4/1.72
M17	13.85/1.72
M18, M19, M20, M21,M22	0.72/0.72

Table 2: Aspect ratios of the MOS transistors of Fig. 2 [29]

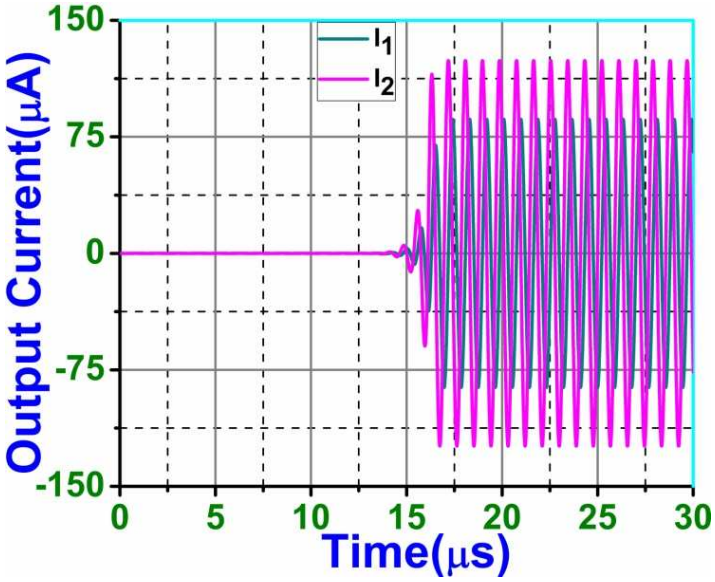


(a)

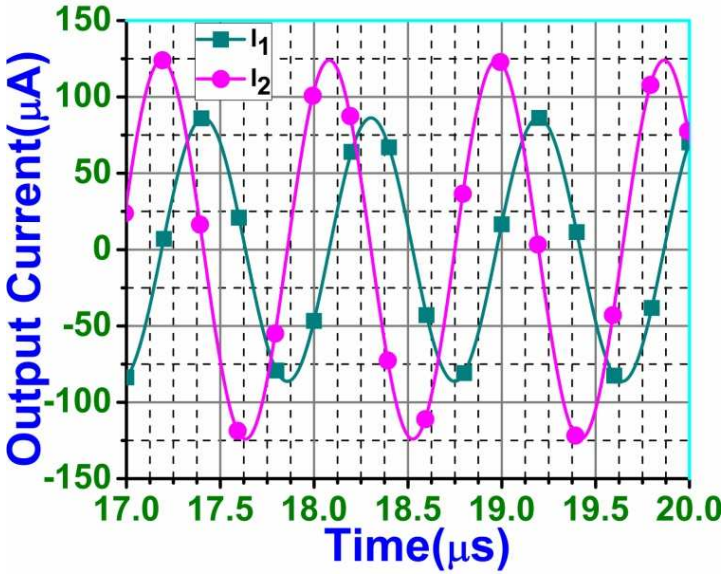


(b)

Figure 6: (a) Initial and (b) steady state waveforms of the quadrature voltage outputs



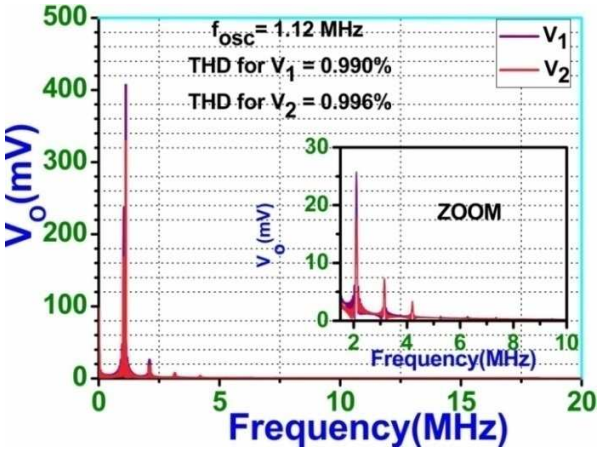
(a)



(b)

Figure 7: (a) Initial and (b) steady state waveforms of the quadrature current outputs

The frequency spectrum of V_1, V_2 and I_1, I_2 are depicted in Fig. 8a and Fig. 8b respectively. Fig. 8 shows that the total harmonic distortions (THDs) for all current and voltage outputs are within 1%. The plot of V_1vs V_2 and I_1vs I_2 in X-Y plane is given in Fig. 9a and Fig. 9b respectively. Fig. 9 confirms about the quadrature relationship between the simulated outputs. The variation of the oscillation frequency (f_o) with respect to the variation of the capacitor C_2 is displayed in Fig. 10. Static power dissipation by the reported circuit is found to be 1.35 mW.



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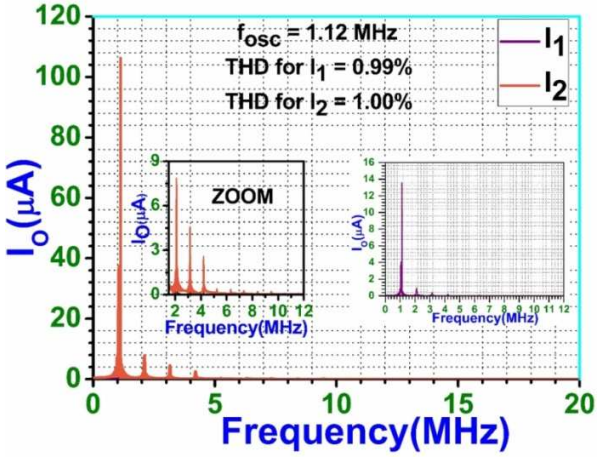
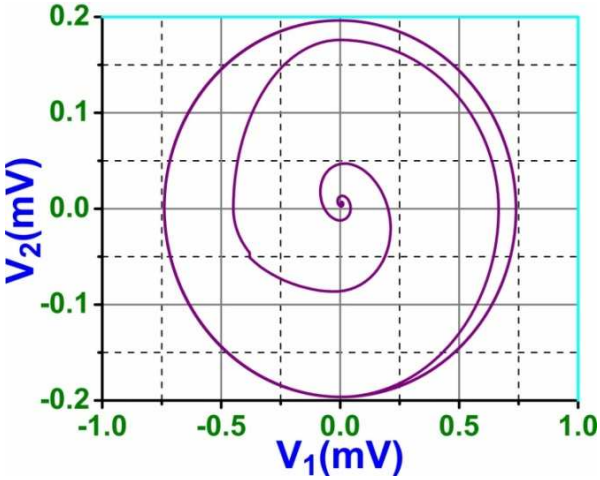
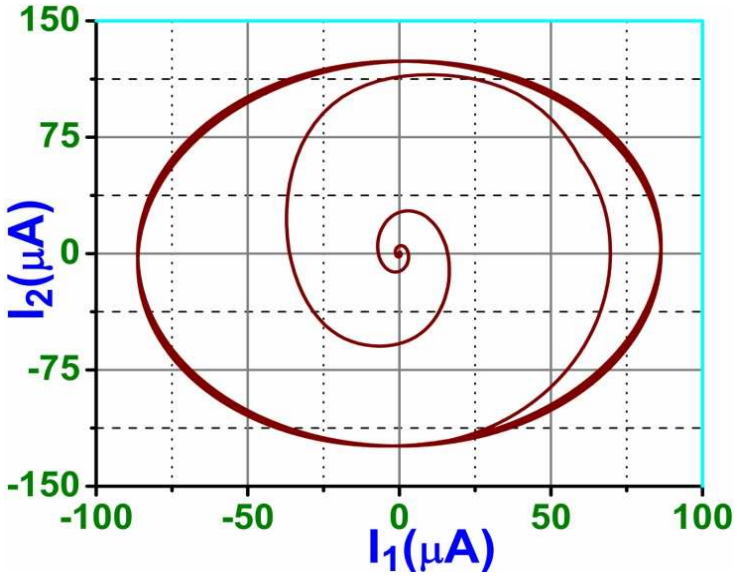


(b)

Figure 8: Frequency spectrum of (a) V_1, V_2 and (b) I_1, I_2



(a)



(b)

Figure 9: Lissajous figure showing quadrature relationship between (a) voltage V_1 and V_2 and (b) current I_1 and I_2

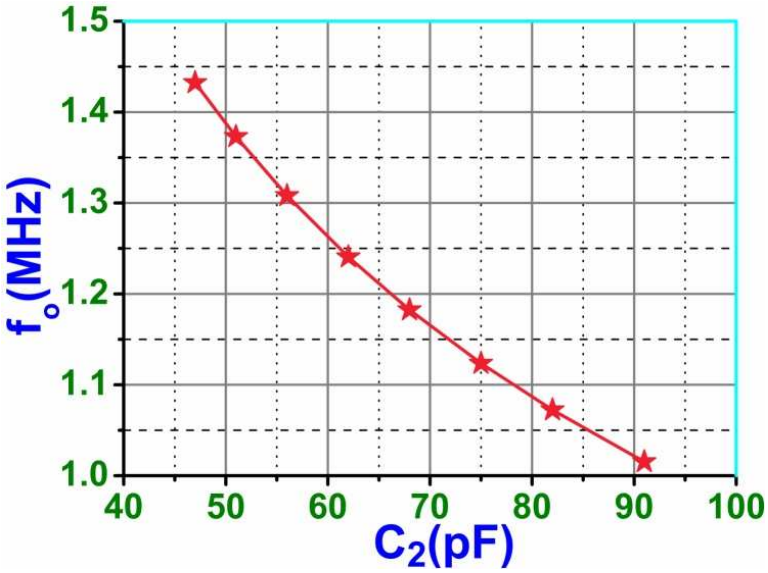


Figure 10: Variation of f_0 with respect to C_2

Monte-Carlo simulation for 100 samples with 5% tolerance in the value of R_2, R_3 and C_3 has been performed to verify the robustness of the proposed oscillator circuit. The result has been given in Fig. 11. The result shows that the oscillation frequency varies from 1.10635 MHz to 1.12820 MHz with mean value 1.11744 MHz and standard deviation 5.18351 kHz. Thus the shift in frequency is less than 1% on both side of mean value.

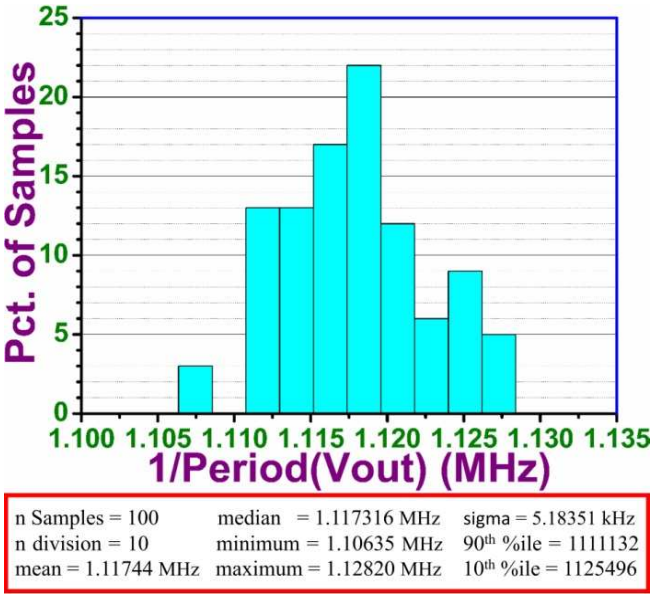


Figure 11: Monte-Carlo simulation result

6. Conclusion

A new third-order quadrature oscillator circuit using two VDCC, three grounded capacitors, and three resistors (two are grounded) is presented in this manuscript. The oscillation condition and oscillation frequency of the proposed quadrature oscillator are independently controllable by single grounded passive component, as well as electronic tuning is also possible. The circuit is feasible for IC fabrication, as all the capacitors are grounded. Both current-mode and voltage-mode quadrature signals can be simultaneously obtained in the reported circuit. PSPICE simulation results have confirmed the workability of the circuit. THD is within 1%. Static power dissipation is about 1.35 mW. Monte-Carlo simulation result has been included.

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