2018

MCA 1st Semester Examination

DIGITAL LOGIC LAB.

PAPER—MCA-191

(Practical)

Full Marks : 100

Time : 3 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer any *two* questions (Lottery basis). 2×35

1. Design and implement a full adder circuit using NAND gates only.

2. Design and implement a 8 bit parity generator.

3. Design and implement a 4 bit adder/subtractor using flip-flop.

4. Design and implement a 2 bit digital comparator.

5. Design and implement a BCD to excess 3 code converter using full adder.

6. Design and implement a half-subtractor circuit using NAND gates only.

7. Design and implement a full subtractor circuit.

8. Design and implement a D flip-flop.

9. Design and implement a J–K flip-flop.

10. Design and implement a 4 bit ripple counter.

11. Design and implement a mod-10 counter.

12. Design and implement a 4 bit right shift register.

13. Design and implement a 4 bit left shift register.

14. Design and implement a 4 bit ring counter.

15. Design and implement a J–K master slave flip-flop.

Practical Note Book : 10

Viva-Voce : 20
