2018

MCA 1st Semester Examination

DIGITAL LOGIC & DESIGN

PAPER—MCA-103

Full Marks : 100

Time : 3 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer any *seven* questions. 7×10

1. (a) Convert binary $(10110)_2$ to gray code.

(b) Convert hexadecimal number $(E7F6)_{16}$ to its decimal equivalent.

(c) Convert graycode 1101 to its BCD number.

(d) Add two BCD numbers
$(1001\ 110)_{BCD}$ and $(0001\ 1000)_{BCD}$.

(e) $(436)_{10} = (?)_8$

2. (a) Simplify $F(W, X, Y, Z) = \Sigma_m(3, 4, 5, 7, 9, 13, 14, 15)$ using K-map in SOP form.

(b) Find all prime implicants and essential prime implicants for $F(A, B, C, D) = \Sigma_m (0, 2, 3, 8, 9, 10, 11, 12, 13, 14, 15)$

5+5

3. (a) Consider the following boolean expresion

$$F = BD + A\bar{B}C + A\overline{B\bar{D}} + AB\bar{C}\ .$$

Calculate literal cost, gate input cost and gate input cost with NOTs.

(b) Implement $F(A, B, C) = \Sigma(1, 3, 5, 6)$ with a multiplexer.

4+6

4. (a) Design a 5×32 decoder using 2×4 and 3×8 decoders.

(b) Design a full subtractor using two half-subtractors.

5+5

5. (a) What is the difference between set-up time and hold time ?

(b) What is propagration delay ?

(c) Explain edge triggered J-K flip-flop with circuit diagram.

3+2+5

6. (a) What are the functions of preset and clear of a flip-flop ?

(b) Explain D flip-flop with diagram.

(c) What is the advantage and disadvantage of D flip-flop ?

3+5+2

7. (a) What is counter ? Compare synchronous and asynchronous counter.

(b) Explain ripple counter with circuit diagram. 4+6

8. (a) Draw and explain a 4 bit adder-subtractor using full adder.

(b) What is decoder ? Draw and explain a 3 to 8 line decoder.

5+5

9. (a) What is race condition ? When does it occur ?

(b) What is propagation delay ?

(c) Differentiate between edge triggering and level clocking.

4+2+4

[*Internal Assessment : 30*]
