2018

M.Sc.

2nd Semester Examination

ELECTRONICS

PAPER—ELC-205

Subject Code—27

(Practical)

Full Marks : 50

Time : 3 Hours

The figures in the right-hnad margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

(*Digital Electronics Lab.*)

Answer any *one* question selecting it by a lucky draw.

1. Design a 2-bit comparator circuit. Compare two bit binary number and show results.

2. Design circuits to convert BCD to gray code and gray to BCD code. Tabulate results.

3. Design half adder and full adder circuit. Realise by basic gates and also by MUX.

4. Design half adder and Full adder circuit. Realise by NAND gates and also by 4 : 1 MUX.

5. Design half substractor and full substractor circuit. Realise the circuit by basic gates and by 4 : 1 MUX.

6. Design a half substractor and full substractor circuit. Realise it any NAND gates only. Use MUX to implement the half substractor and full substractor.

7. Design a JK and MS flip using universal gates. Realise its truth table. Convert the Ms flip-flop to D and T type flip-flop and realise truth table.

8. Design a MOD-10 synchronous counter. Show its counting states.

9. Design a MOD-10 ripple counter. Show its counting states.

10. Design a random counter which will count following states :

(1, 3, 5, 7, 0, 2, 4)

11. Design a astable multivibrator using 555 timer for two different duty cycles. Duty cycles to be provided in the examination hall.

12. Design a 4-bit R-2R ladder D/A converter.

13. Design a 3-bit R-2R ladder D/A converter.

Distribution of Marks

Theory	:	10 Marks
Circuit (Implementation)	:	10 Marks
Experiment	:	05 Marks
Results and discussion	:	10 Marks
Viva-Voce	:	10 Marks
Lab. Note Book	:	05 Marks
Total	:	50 Marks