2018

M.Sc.

2nd Semester Examination

ELECTRONICS

PAPER—ELC-203

Subject Code—27

Full Marks : 50

Time : 2 Hours

The figures in the right-hand margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

(Digital Electronics and Mobile Communication)

Answer Q. No. *1* and any *three* from the rest.

1. (a) Which logic is the fastest and why ?

(b) Using 4 : 1 MUX, implement the logic function

$F(A,B,C) = \Sigma m(1,2,4,7)$

(c) Write down the characteristic equation of a JK F/F.

(d) A 6bi DAC has a step size of 50 mv. Determine the full scale output voltage and the percentage resolution.

(e) What is frequency reuse in wireless communication ?

5×2

2. (a) Differentiate between combinational circuits and sequential circuits.

(b) Convert JK F/F to T F/F.

(c) Design two bit ripple counter and show its timing diagram.

2+4+4

3. (a) Implement logic function $F = \overline{A(BC + D)}$ by using CMOS logic.

(b) By using circuit diagram explain two input TTL NAND gate.

(c) Write two advantages of CMOS logic families.

3+5+2

4. (a) Calculate the output voltage (V_{out}) when the input is 0100 by using R-2R lader type DAC.

   (b) Write short notes on successive approximation type ADC converter. 5+5

5. (a) Mention different layers used in OSI model and briefly describe them.

   (b) Briefly discuss about HLR and VLR in mobile communication. 6+4

6. (a) By using proper circuit diagram, explain monostate operation.

   (b) Design Johnson counter and mention its states. 6+4

[Internal Assessment — 10 Marks]

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