PG/IIIS/ELC-303/18

M.Sc. 3rd Semester Examination, 2018

ELECTRONICS

(VLSI Engineering)

PAPER – ELC-303

Full Marks : 50

Time : 2 hours

Answer **Q.No.1** and any **three** questions from the rest

The figures in the right hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

1. Answer the followings : 2 × 5

(*a*) Draw and explain Y-chart.

(*b*) Discuss the layout design rules.

(*c*) What is a two-step diffusion process ?

(*d*) Why is the choice of crystal orientation is critical for MOS devices ?

(*e*) What is a MOS switch ?

2. (*a*) Define a class 10 clean room. If we expose a 300-mm water for 1 minute to an air steam under on laminar flow condition at 45 m/min, how many dust particles will deposit on the water in a class 10 clean room ?

(*b*) Mention the different lithographic techniques used in different VLSI technology. Compare them. (2 + 2) + (2 + 4)

3. (*a*) What are the advantages of an ion implantation over a diffusion process ? Describe an ion implantation system with a schematic diagram.

(*b*) Explain the projected range and projected straggle of ion implantation. Assume 100-KeV boron implants on a 200-mm silicon water at a dose of 5×10^{14} ions/cm^2.

Calculate the peak concentration and required ion beam current for 1 minute of implantation.

(Given 0·31 and 0·07 μm for projected range and projected straggle respectively)

$(2 + 3) + (2 + 1\frac{1}{2} + 1\frac{1}{2})$

4. (*a*) What is a stick diagram ? Draw a stick diagram of Fig. 1 :

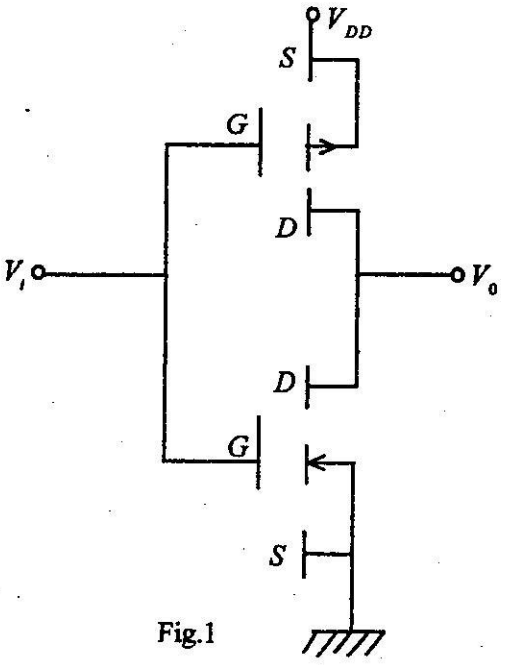

Fig.1

(*b*) Translate the Fig.1 into a monolithic IC clearly describing different steps. (2 + 2) + 6

5. (*a*) Draw the two-stage CMOS OPAMP circuit and explain its working principle.

(*b*) Why is compensation used in CMOS OPAMP ? Draw the two-stage CMOS OPAMP circuit with compensation. (2 + 3) + (3 + 2)

6. (*a*) Explain CMOS logic design. A logic gate has $V_{OH} = 5V$, $V_{OL} = 0{\cdot}2$ V, $V_{IH} = 2{\cdot}5$ V, and $V_{IL} = 0{\cdot}8$ V. Calculate the noise margin. (symbols have their usual meanings).

(*b*) Implement the function
$F = \Sigma m\,(0, 1, 2, 4, 6, 8, 10, 12, 14)$
using CMOS logic. (3 + 2) + 5

[*Internal Assessment* : 10 Marks]