NEW

2016

BCA

1st Semester Examination

DIGITAL ELECTRONICS LAB

PAPER—1197 (Set-2)

(PRACTICAL)

Full Marks : 100

Time : 3 Hours

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Illustrate the answers wherever necessary.

Answer any *two* questions taking *one* from each group (*Lottery Basis*). 2×30

Group—A 1×30

1. Design a Full adder using NAND gates and verify the truth table.

2. Design Basic gates using minimum NOR gates.

3. Design a half subtractor using NAND gates and verify the truth table.

4. Design gray code to BCD converter and verify the truth table.

5. Design a 4 : 1 MUX using the NOR gates and verify the truth table.

6. Design an excess – 3 to BCD converter circuit and verify its truth table.

7. Implement $Y = (X + Z).(\overline{X} + Y)$ using Basic gates and verify its truth table.

8. Design 2 bit comparators circuit using suitable gates and verify its truth table.

9. Design 8 to 3 encoder circuit and verify its result.

10. Design a 4 bit 2's complement subtractor using necessary gates.

11. Design a 2's complement subtractor (4-bit) using IC 7483 and XOR gates.

12. Design a 2 bit comparator and verify the truth table.

13. Design a circuit to convert BCD to excess–3.

14. Simplify the following fuction using K-map and implement using basic gates.

$$G = \sum m(0, 5, 7, 13, 14, 15)$$

15. Design XOR, XNOR, OR and AND gates using NOR gates only. 30

16. Design a half subtractor using NAND gate and also design a full subtractor using two half-subtractors. 15+15

17. Design a 3 to 8 decoder and verify its result. 15+15

18. Design a 1 : 4 DEMUX and verify its truth table. 30

19. Design a gray code to BCD converter and verify the truth table.

20. Design a half adder using NOR gates and also design full adder using two half-odders. 15+15

Group—B 1×30

1. Design J-K master slave F/F and verify its execution table.

2. Construct clocked S-R F/F using NAND gates and verify its operation.

3. Design a 4 bit biderectional shift register.

4. Design 4 bit ripple counter using J-K F/F.

5. Design asynchronous up-counter of MOD 10 counter.

6. Design 4 bit SISO Register using D F/F and verify the output.

7. Design OR operation using DTL and establish its truth table.

8. Design a asynchronous up counter of MOD 5.

9. Design and implement right shift register and verify the output.

10. Design D F/F using NAND gates and verify its output.

11. Design a synchronous counter which cycles through $7 \rightarrow 3 \rightarrow 4 \rightarrow 0 \rightarrow 5 \rightarrow 7$ using J-K flip-flop and verify it. 30

12. Design a Buffer register and show the following result :

Input = 1010

Output = 1010

13. Design a ripple counter using J-K flip-flop. 30

14. Design a J-K master slave flip-flop and verify its result. 30

15. Design a 4 bit bidirectional shift register. 30

16. Design asynchronous up counter of the following MOD using IC-7476. 30

(i) MOD 10 (ii) MOD 5

17. Design a clocked SR and J-K flip-flop with preset and clear using NAND gates only. 30

18. Design a 4 bit bidirectional shift register. 30

19. Design AND and OR operation using DTL and establish its truth table. 30

20. Construct astable multivibrator using IC 555 timer. Measure its frequency and duty cycle by CRO.

INSTRUCTIONS

Distribution of Marks :

Theory	:	*10*
Circuit	:	*05*
Implementation	:	*10*
Verification	:	*05*
	Total :	*30*

Viva — *05*

PNB — *05*

[Internal Assessment — 30]